UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

ACQIS LLC, a Texas limited liability company, Plaintiff, v. INVENTEC CORPORATION, a Taiwan corporation, Defendant.	**Civil Action No.** 6:20-CV-00965 **JURY TRIAL DEMANDED**

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff ACQIS LLC ("Plaintiff" or "ACQIS"), by its attorneys, hereby alleges patent infringement against Defendant Inventec Corporation ("Defendant" or "Inventec") as follows:

INTRODUCTION

1. This is an action for patent infringement under the United States Patent Laws, 35 U.S.C. § 1 *et seq.* Beginning in the late 1990s, Dr. William Chu founded ACQIS and invented a variety of pioneering computer technologies that employed serial transmission along low voltage differential signal (LVDS) channels to dramatically increase the speed at which data can be transmitted while also reducing power consumption and noise. Dr. Chu's inventions have become foundational in the computer industry, and are found in a variety of data transmission systems, including PCI Express (PCIe) and/or USB 3.x[1] transactions.

2. Inventec has infringed and continues to infringe, directly and/or indirectly, the following patents owned by ACQIS: U.S. Patent Nos. 9,529,768 ("'768 patent"), 9,703,750 ("'750

[1] As used herein, "USB 3.x" refers to USB 3.0 and subsequent versions, including USB 3.1, USB 3.2, and any other subsequent versions.

patent"), 8,977,797 ("'797 patent"), 8,756,359 ("'359 patent"); RE44,654 ("'654 patent"); RE44,739 ("'739 patent"); RE43,602 ("'602 patent"); and RE42,984 ("'984 patent") (collectively, the "ACQIS Patents"). Copies of the ACQIS Patents are attached to this Complaint as **Exhibits 1-8**.

3. Specifically, Inventec has directly and/or indirectly infringed and continues to infringe the ACQIS Patents through: (1) the manufacture, use, offering for sale, and/or sale in the United States, and/or the importation into the United States, of infringing computer products; (2) the practice of claimed methods of the ACQIS Patents by using and/or testing computer products in the United States; (3) the importation into the United States of computer products made abroad using ACQIS's patented processes; and (4) the inducement of third parties to engage in, and/or contributing to the engagement of third parties in, the activity described above with knowledge of the ACQIS Patents and of the third parties' infringing actions.

4. ACQIS seeks damages and other relief for Inventec's infringement of the ACQIS Patents. ACQIS is entitled to past damages because, without limitation, it has provided actual notice to Inventec and for method claims which do not require marking.

THE PARTIES

5. Plaintiff ACQIS LLC, is a limited liability company organized and existing under the laws of the State of Texas, with offices at 411 Interchange Street, McKinney, Texas 75071. A related entity, ACQIS Technology, Inc., is a corporation organized under the laws of the State of Delaware, having its principal place of business at 1503 Grant Road, Suite 100, Mountain View, California 94040. ACQIS LLC is operated from California, where its President, Dr. William Chu, resides. Dr. Chu is also the Chief Executive Officer of ACQIS Technology, Inc.

6. Defendant Inventec is a Taiwan corporation with its global headquarters located at No. 66, Hougang St., Shihlin Dist., Taipei City, TW-11170, Taiwan, R.O.C.

7. Defendant has a distribution chain (together with other Inventec subsidiaries, affiliates, and intermediaries) with respect to the manufacture, use, offering to sell, and/or sale of infringing computer products and with respect to the importation into the United States of infringing computer products and of computer products made abroad using patented processes claimed in the ACQIS Patents.

JURISDICTION AND VENUE

8. This is an action for patent infringement under the United States patent laws, 35 U.S.C. § 101 *et seq*.

9. This Court has subject matter jurisdiction pursuant to 28 U.S.C. §§ 1331 and 1338(a).

10. This Court has specific and personal jurisdiction over the Defendant consistent with the requirements of the Due Process Clause of the United States Constitution and the Texas Long Arm Statute. On information and belief, Defendant has purposefully manufactured and/or distributed computer products that infringe the ACQIS Patents, or that were made abroad using patented processes claimed in the ACQIS Patents, through established distribution channels with the expectation that those products would be sold in the United States, State of Texas, and in this District. Further, Defendant has (itself and/or through the activities of subsidiaries, affiliates, or intermediaries) committed and continues to commit acts of patent infringement in the United States, State of Texas and this District, including by making, using, offering to sell, and/or selling infringing computer products in the United States, State of Texas and this District; importing infringing computer products and/or computer products made abroad using ACQIS's patented processes into the United States for sale in the State of Texas and this District; and/or inducing others to commit acts of patent infringement in the United States, State of Texas and this District. Accordingly, Inventec has established minimum contacts within Texas and purposefully availed itself of the benefits of Texas, and the exercise of personal jurisdiction over Inventec would not offend traditional

notions of fair play and substantial justice. In addition, or in the alternative, this Court has personal jurisdiction over Inventec pursuant to Federal Rule of Civil Procedure 4(k)(2).

11. Inventec conducts business in the United States, the State of Texas and this District through subsidiaries, affiliates, and intermediaries, including regional offices in Silicon Valley, in Houston, and in this District in Austin.

12. Venue is proper in this District pursuant to 28 U.S.C. § 1391(c)(3) because Defendant does not reside in the United States and thus may be sued in any judicial district in the United States.

FACTUAL BACKGROUND

Dr. Chu and the ACQIS Patents

13. Dr. William Chu has been a prolific innovator in the computing industry since the 1970s.

14. In 1976, Dr. Chu received his Ph.D. in Electrical Engineering from the University of California, Berkeley.

15. Dr. Chu then began working in semiconductor design for American Microsystems, Inc. from 1976 to 1977, and then for Zilog, Inc. from 1977 to 1982.

16. In 1982, Dr. Chu founded Verticom, Inc., which developed innovative technologies relating to video transmission over telephone lines. Verticom also developed graphics products for the PC computer-aided design (CAD) market. Verticom's success resulted in its stock being listed on the NASDAQ exchange in 1987. In 1988, Verticom was acquired by Western Digital Imaging, Inc.

17. Dr. Chu served as Vice President of Engineering for Western Digital from 1988 to 1991, overseeing a development team in the desktop and portable graphics chip division. In the course of his work at Western Digital, Dr. Chu in 1988 started the company's portable graphics chip business, which became #1 in the portable graphics chip market by 1991. Dr. Chu also led Western Digital to achieve the #1 market share in the PC graphics market in 1990.

18. After Western Digital, Dr. Chu worked for Acumos, Inc. from 1991 to 1992 as a Vice President managing engineering for computer graphics chip development. Acumos was acquired by Cirrus Logic, Inc. in 1992.

19. Dr. Chu then worked for Cirrus Logic from 1992 to 1997, first as a General Manager in the Desktop Graphics Division and later as Co-President of the Graphics Chip Business Unit. During Dr. Chu's time at Cirrus Logic, the company achieved #1 market share in the PC graphics chip market.

20. In 1998, Dr. Chu founded ACQIS Technology, Inc. to pursue his vision of developing a small, portable computer module that could be interchangeably connected with a variety of different peripheral consoles. In the course of this development effort, Dr. Chu recognized the need for a better interconnection between the core computing module and a peripheral console. Such interconnections traditionally conveyed peripheral component interconnect (PCI) bus transactions in parallel using a large number of signal channels and connector pins. This made it difficult to employ LVDS channels, which are more "cable friendly," consume less power, and generate less noise. Dr. Chu wanted to develop an interconnection system that was scalable, used connectors with low pin counts, was power-efficient, high performing, and easily extendible for future computing needs and technologies. This development work resulted in a large family of patents now owned by ACQIS, which disclose and claim a variety of pioneering inventions relating to improved, high-performance and low power consuming interconnection technologies for computer modules.

21. After several decades in the industry, Dr. Chu is now a named inventor of approximately forty-one (41) U.S. Patents.

22. Among the patent portfolio covering Dr. Chu's inventions and owned by ACQIS are the ACQIS Patents asserted in this case.

23. The ’768 patent, entitled “Computer System Including CPU or Peripheral Bridge Directly Connected to a Low Voltage Differential Signal Channel that Communicates Serial Bits of a Peripheral Component Interconnect Bus Transaction in Opposite Directions,” was duly and legally issued on December 27, 2016, from a patent application filed March 13, 2014, with William W.Y. Chu as the sole named inventor. The ’768 patent claims priority to U.S. Provisional Patent Application No. 60/134,122, filed on May 14, 1999.

24. The ’750 patent, entitled “Computer System Including CPU or Peripheral Bridge Directly Connected to a Low Voltage Differential Signal Channel that Communicates Serial Bits of a Peripheral Component Interconnect Bus Transaction in Opposite Directions,” was duly and legally issued on July 11, 2017, from a patent application filed October 9, 2014, with William W.Y. Chu as the sole namedinventor. The ’750 patent claims priority to U.S. Provisional Patent Application No. 60/134,122, filed on May 14, 1999.

25. The ’797 patent, entitled “Method of Improving Peripheral Component Interface Communications Utilizing a Low Voltage Differential Signal Channel,” was duly and legally issued on March 10, 2015, from a patent application filed October 10, 2012, with William W.Y. Chu as the sole named inventor. The ’797 patent claims priority to U.S. Provisional Patent Application No. 60/134,122, filed on May 14, 1999.

26. The ’359 patent, entitled “Computer System Including CPU or Peripheral Bridge to Communicate Serial Bits of Peripheral Component Interconnect Bus Transaction and Low Voltage Differential Signal Channel to Convey the Serial Bits,” was duly and legally issued on June 17, 2014, from a patent application filed January 17, 2013, with William W.Y. Chu as the sole named inventor. The ’359 patent claims priority to U.S. Provisional Patent Application No. 60/134,122, filed on May 14, 1999.

27. The ’654 patent, entitled “Data Security Method and Device for Computer Modules,” was duly and legally issued on December 17, 2013, from a reissue application filed October 10, 2012, with William W.Y. Chu as the sole named inventor. The ’654 patent is a reissue of U.S. Patent No. 6,643,777, which issued on November 4, 2003, from a patent application filed May 14, 1999. The ’654 patent claims priority to U.S. Patent Application No. 09/312,199, filed on May 14, 1999.

28. The ’739 patent, entitled “Data Security Method and Device for Computer Modules,” was duly and legally issued on January 28, 2014, from a reissue application filed May 21, 2013, with William W.Y. Chu as the sole named inventor. The ’739 patent is a reissue of U.S. Patent No. 6,643,777, which issued on November 4, 2003, from a patent application filed May 14, 1999. The ’739 patent claims priority to U.S. Patent Application No. 09/312,199, filed on May 14, 1999.

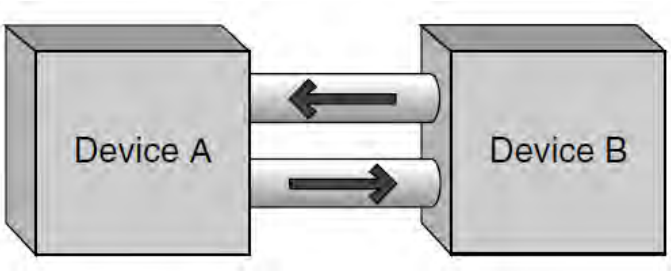
29. The ’602 patent, entitled “Data Security Method and Device for Computer Modules,” was duly and legally issued on August 21, 2012, from a reissue application filed November 10, 2011, with William W.Y. Chu as the sole named inventor. The ’602 patent is a reissue of U.S. Patent No. 6,643,777, which issued on November 4, 2003, from a patent application filed May 14, 1999. The ’602 patent claims priority to U.S. Patent Application No. 09/312,199, filed on May 14, 1999.

30. The ’984 patent, entitled “Data Security Method and Device for Computer Modules,” was duly and legally issued on November 29, 2011, from a reissue application filed September 16, 2009, with William W.Y. Chu as the sole named inventor. The ’984 patent is a reissue of U.S. Patent No. 6,643,777, which issued on November 4, 2003, from a patent application filed May 14, 1999. The ’984 patent claims priority to U.S. Patent Application No. 09/312,199, filed on May 14, 1999.

31. The inventions claimed in the ACQIS Patents enable computers to operate faster with better efficiency through faster interconnections including between the core computing power modules and any connected peripherals.

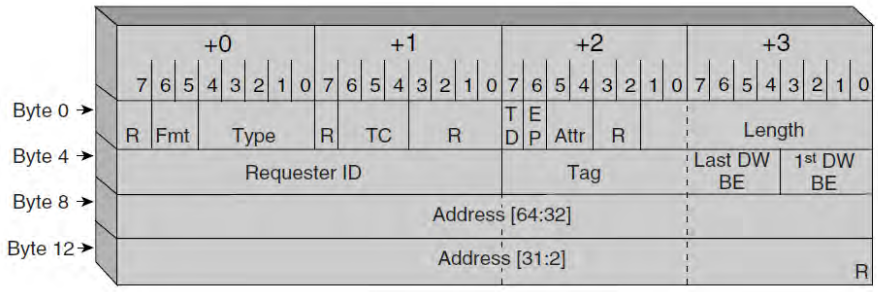
32. The claims in the ACQIS Patents generally relate to computers and computer systems that employ CPUs coupled to LVDS channels that convey various types of data (*e.g.*, PCI bus transactions, USB 3.x data, and/or digital video data) in a serial bit stream using pairs of unidirectional channels to convey the data in opposite directions.

33. Over the years, Dr. Chu's inventive developments have become more and more widely used in computing technologies. One prime example is the computing industry's adoption of PCI Express, which post-dates Dr. Chu's inventions but embodies Dr. Chu's patented interconnection invention by using "high speed, low voltage, differential serial pathway for two devices … to communicate simultaneously by implementing dual unidirectional paths between two devices[.]"



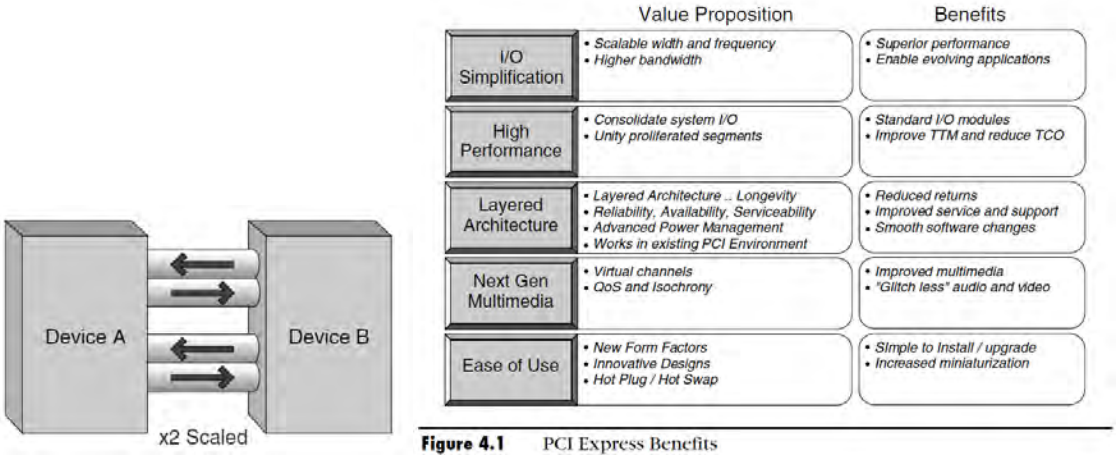
See Introduction to PCI Express – A Hardware and Software Developers Guide, Intel Press (2003), at 1-2 ("There are certain times in the evolution of technology that serve as inflection points that forever change the course of events. For the computing sector and communications, the adoption of PCI Express, a groundbreaking new general input/output architecture, will serve as one of these inflection points.").

34. PCI Express connections transmit data packets known as transaction layer packets (TLP) that include data bits, address bits, and byte enable (BE) information bits.



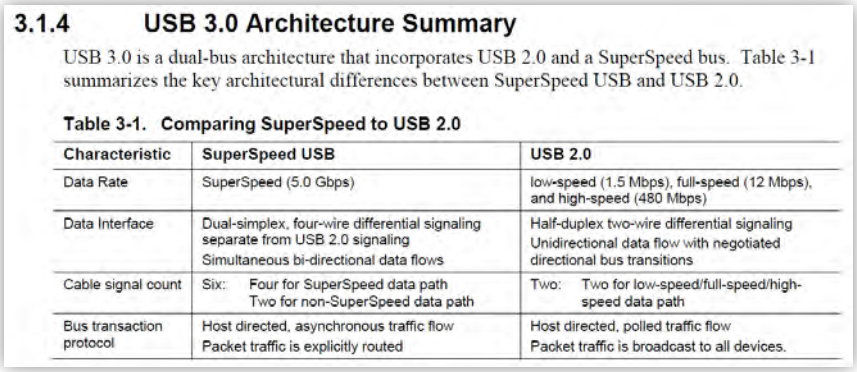
Id. at 93-114.

35. In sum, PCI Express connections are LVDS channels that convey data bits, address bits, and byte enable information bits of a PCI bus transaction in a serial bit stream using pairs of unidirectional, differential signal lanes to convey the information in opposite directions, allowing the connection to be scalable and dramatically reducing the pin-count required for connectors, as well as other benefits.



Id. at 3, 50.

36. Another example of a computer-to-peripheral interconnection that embodies Dr. Chu's patented invention is the USB 3.x connection. The "Super Speed" USB 3.0 architecture uses at least two pairs of unidirectional, point-to-point differential signal paths. Each pair includes a transmit path and a receiving path, thus transmitting the USB data packet information in opposite directions.



3.1.4 USB 3.0 Architecture Summary

USB 3.0 is a dual-bus architecture that incorporates USB 2.0 and a SuperSpeed bus. Table 3-1 summarizes the key architectural differences between SuperSpeed USB and USB 2.0.

Table 3-1. Comparing SuperSpeed to USB 2.0

Characteristic	SuperSpeed USB	USB 2.0
Data Rate	SuperSpeed (5.0 Gbps)	low-speed (1.5 Mbps), full-speed (12 Mbps), and high-speed (480 Mbps)
Data Interface	Dual-simplex, four-wire differential signaling separate from USB 2.0 signaling Simultaneous bi-directional data flows	Half-duplex two-wire differential signaling Unidirectional data flow with negotiated directional bus transitions
Cable signal count	Six: Four for SuperSpeed data path Two for non-SuperSpeed data path	Two: Two for low-speed/full-speed/high-speed data path
Bus transaction protocol	Host directed, asynchronous traffic flow Packet traffic is explicitly routed	Host directed, polled traffic flow Packet traffic is broadcast to all devices.

Universal Serial Bus 3.0 Specification, Rev. 1.0 (Nov. 12, 2008), at 3-1 to 3.5. In sum, USB 3.x connections are LVDS channels using two unidirectional, differential signal pairs that transmit USB protocol data packets in opposite directions.

37. Intel's Direct Media Interface (DMI) channel is similar to PCIe and implements four serial lanes that all use differential signaling constituting 2 transmit lanes and 2 receive lanes and, therefore, transmitting data in opposite directions. *See* https://www.intel.com/content/dam/www/public/us/en/documents/white-papers/ia-introduction-basics-paper.pdf. *See also* https://en.wikipedia.org/wiki/Direct_Media_Interface ("DMI shares many characteristics with PCI Express, using multiple lanes and differential signaling to form a point-to-point link.").

38. Each claim of the ACQIS Patents is a patentable, valid, and enforceable invention that is novel and non-obvious over the prior art.

39. ACQIS has not authorized or licensed Inventec to practice any of the inventions claimed in the ACQIS Patents.

Inventec's Infringing Products

40. Inventec manufactures and sells computers, telephones, notebooks, servers, and motherboards on a global scale. Inventec imports infringing computer servers and motherboards, and computer servers and motherboards made using infringing processes, into the United States through

established distribution channels with the expectation that those products would be sold in the United States, State of Texas and this District.

41. Inventec has directly infringed, and continues to infringe, one or more claims of each of the ACQIS Patents under at least 35 U.S.C. §§ 271(a) and (g), by making, using, offering to sell, and/or selling within the United States, and/or importing into the United States computer products that embody the claimed inventions of Dr. Chu, and by importing into the United States computer products that were made abroad using patented processes claimed in the ACQIS Patents.

42. Inventec makes, uses, imports, and sells computer servers and motherboards in the United States that infringe one or more of the claims in the ACQIS Patents, and/or imports into the United States computer servers and motherboards that were made abroad using patented processes claimed in the ACQIS Patents, including without limitation servers and related accessories sold under the brand names K-Series, P-Series, and A-Series, and motherboards sold under the brand name B-Series.[2]

43. The Inventec servers fall into one of two categories. Some of the Inventec servers are configured and operate in substantially the same way as the K888G4 – Performance Server System as an example for illustrative purposes. These include, without limitation, K888G4 – Performance Server System and K900G4 – 2U 4-Node HPC Server. Likewise, as shown further below, other Inventec servers are configured and operate in substantially the same way as explained below using the P47G4 – Single-Socket HPC/AI/VDI Server as an example for illustrative purposes. The products described above are collectively referred to as the "Accused Servers."

44. All of the Inventec motherboards are marketed under the brand name B-Series, and include without limitation the B880G4 – Common EATX Motherboard and B888G4 – L-Shape High

[2] Inventec also advertises categories of laptops and desktops that, on information and belief, are likely to infringe the ACQIS Patents. *See* https://www.inventec.com/en/solution.

Density Motherboard. All accused motherboards are configured and operate in substantially the same way as explained below using the B880G4 – Common EATX Motherboard as an example for illustrative purposes. These products are collectively referred to as the "Accused Motherboards."

45. On information and belief, the Accused Servers and Accused Motherboards that Inventec imports into the United States are manufactured outside the United States using one or more processes claimed in the ACQIS Patents.

46. The Accused Servers and Accused Motherboards include products made, used, offered for sale, sold within the United States, and/or imported into the United States at least since ACQIS provided Inventec with actual notice of its infringement on or around May 14, 2018.

47. The Accused Servers and Accused Motherboards also include products made using the processes claimed in the ACQIS Patents and imported into the United States within the six years preceding the date of this Complaint.

48. The Accused Servers and Accused Motherboards also include products that are used to perform one or more methods claimed in the ACQIS Patents within the six years preceding the date of this Complaint.

The Accused Servers

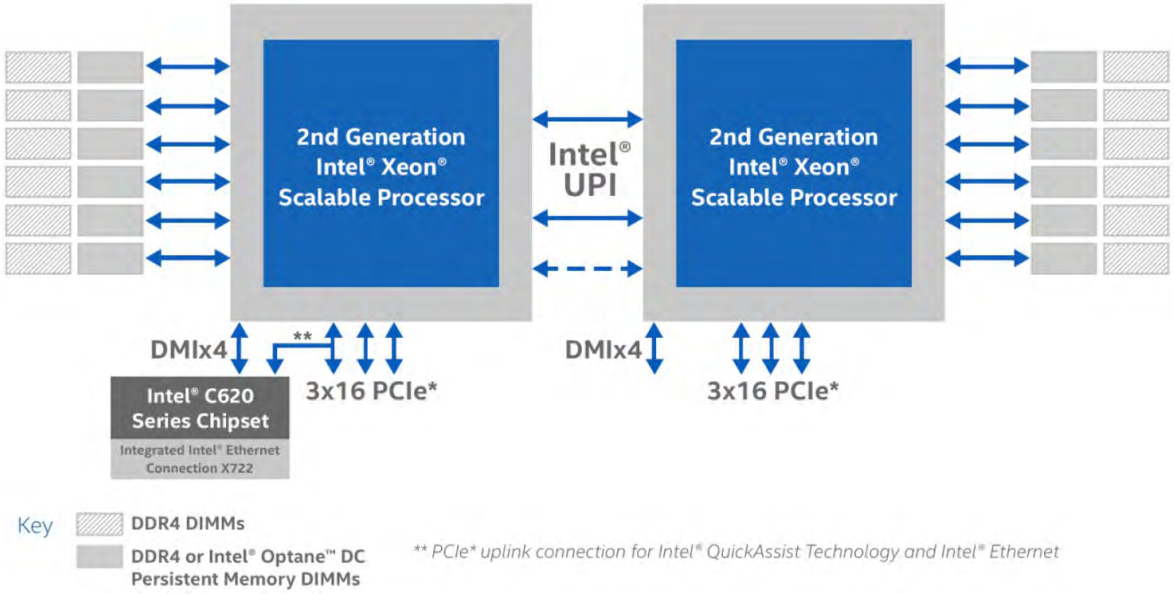
49. The K888G4 – Performance Server System Series is a modular computer system that can run on various server operating systems.

https://ebg.inventec.com/en/product/Server/2U/K888G4

50. The K888G4 – Performance Server System Series uses Intel® Xeon® Processor Scalable Family, which have integrated interface controllers on a single chip to drive the PCIe channels connected to the processor.

Processor	Dual Socket;Intel® Xeon® Processor Scalable Family

https://ebg.inventec.com/en/product/Server/2U/K888G4



https://www.intel.com/content/www/us/en/design/products-and-solutions/processors-and-chipsets/cascade-lake/2nd-gen-intel-xeon-scalable-processors.html

51. The K888G4 – Performance Server System Series includes a variety of connectors that can couple the CPU to a console, including without limitation a power supply:

Form Factor	2U1N rack mount with slide rail W x H x D: 436.9x 86.9x 736.6 mm (17.20x 3.42x 29.00 inch)

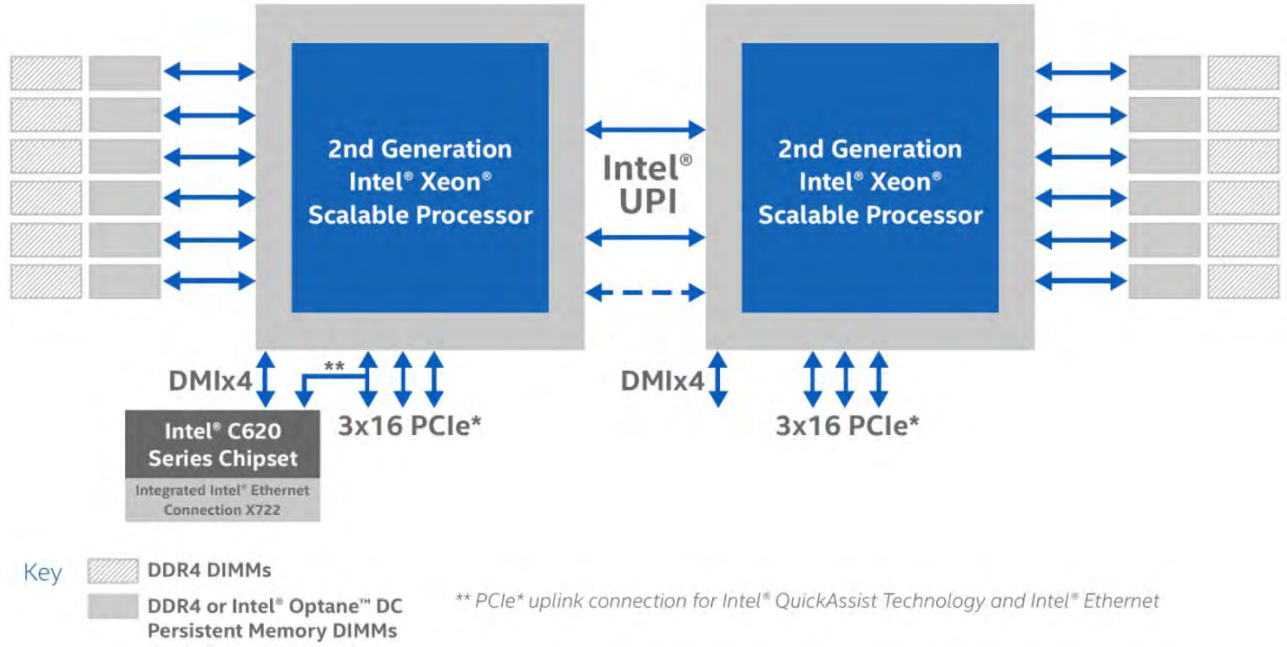
Expansion Slot	Option1: 3x PCIE Gen3 x16 (Low Profile) Option2: 4x PCIE Gen3 x8 (FHFL) 2x PCIE Gen3 x8 (Low Profile) 1x PCIe Gen3 OCP 2.0 A+B NIC mezz 1x Inventec Storage mezz
Power Supply	Option1: 1600W (220V) Platinum (1+1 redundancy) Option2: 800W (110V) Platinum (1+1 redundancy)

https://ebg.inventec.com/en/product/Server/2U/K888G4

52. The Intel processors employed in the K888G4 – Performance Server System directly connect to a variety of LVDS channels that convey data bits in a serial stream using unidirectional pairs of lanes transmitting data in opposite direction, including Intel's DMI and PCIe channels.

> **Great Density and Scalability :** Adopting Intel® C622 chipset, supporting dual Intel® Xeon® Processor Scalable Family and up to 3TB of DDR4 memory. K888G4 series host four PCIe x16 lanes, enabling expansion of up to six PCIe cards with riser boards, and support the latest Intel® technologies, such as Intel® Optane™ Persistent Memory which is ready with 2nd Gen Intel® Xeon® Processor Scalable Family, etc.

https://ebg.inventec.com/en/product/Server/2U/K888G4



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53. The Intel processors employed in the K888G4 – Performance Server System also connect to LVDS channels that convey USB data packets through pairs of unidirectional differential signal paths in opposite directions—USB 3.x ports for external cables.

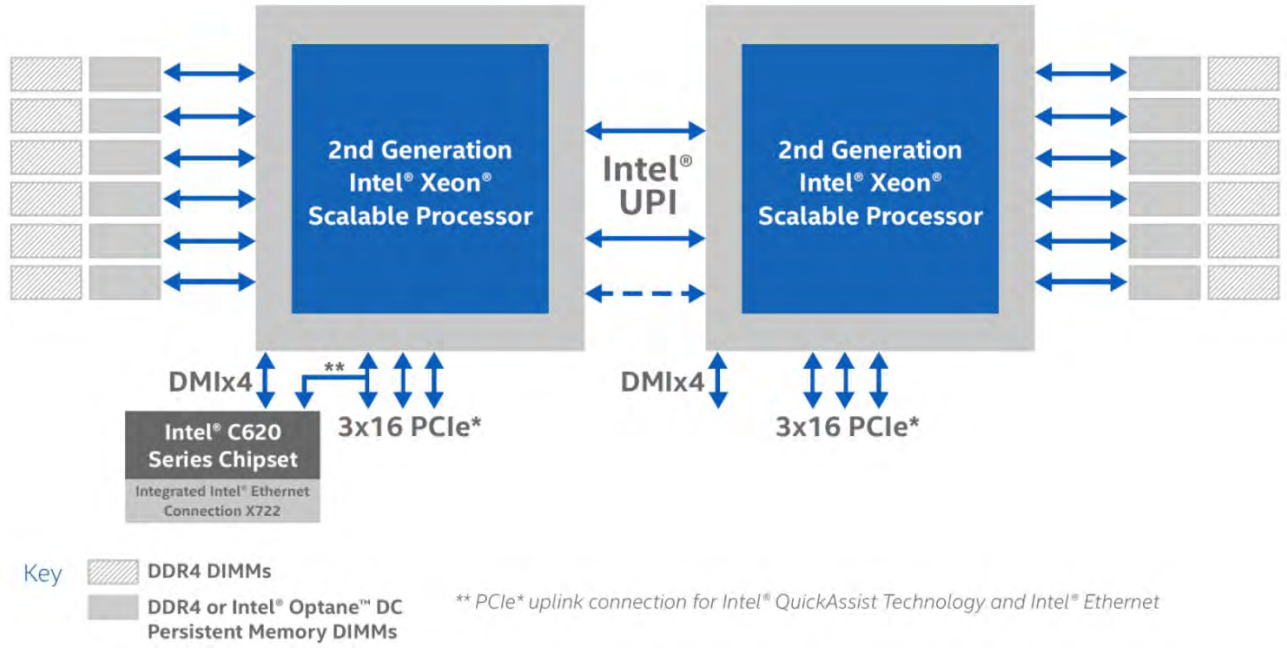
- Supports PCIe*, USB, SATA* and connects to Ethernet, SSD and FPGA peripherals

https://www.intel.com/content/www/us/en/design/products-and-solutions/processors-and-chipsets/cascade-lake/2nd-gen-intel-xeon-scalable-processors.html

54. The K888G4 – Performance Server System has system memory directly coupled to the CPU.

Memory 24x DDR4 DIMM slot

https://ebg.inventec.com/en/product/Server/2U/K888G4



https://www.intel.com/content/www/us/en/design/products-and-solutions/processors-and-chipsets/cascade-lake/2nd-gen-intel-xeon-scalable-processors.html

55. The K888G4 – Performance Server System has a mass storage hard drive coupled to the CPU.

Storage Controller	Onboard: 12x SATA3 6Gb/s port Inventec storage mezz card options: Option1: SAS3-3008-8i (12Gb/s) Option2: SAS3-3216-16i (12Gb/s) Option3: SAS3-3224-24i (12Gb/s) Option4: SAS3-3324-24i (12Gb/s, RAID)

https://ebg.inventec.com/en/product/Server/2U/K888G4

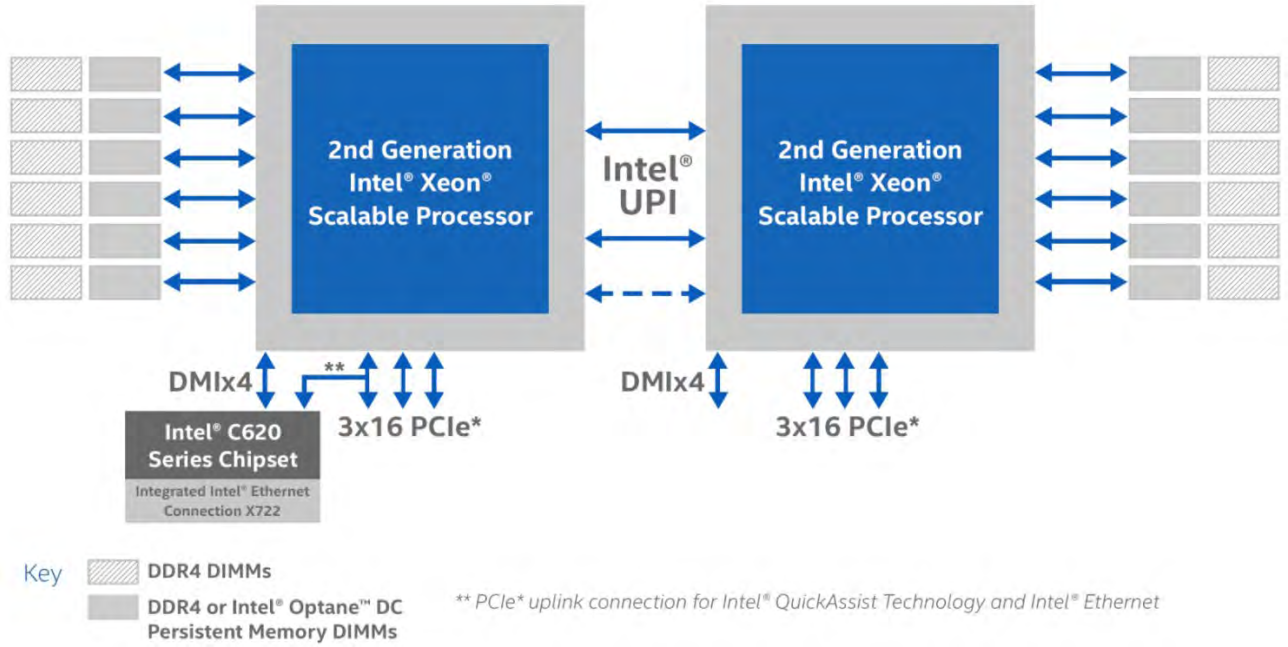
- Supports PCIe*, USB, SATA* and connects to Ethernet, SSD and FPGA peripherals

https://www.intel.com/content/www/us/en/design/products-and-solutions/processors-and-chipsets/cascade-lake/2nd-gen-intel-xeon-scalable-processors.html

56. The Intel processors used in the K888G4 – Performance Server System have a peripheral bridge called the C622 chipset PCH connected to the CPU via the DMI, which has an integrated controller. The C621 Chipset is part of the Intel C620 Series. *See* https://www.intel.com/content/www/us/en/design/products-and-solutions/processors-and-chipsets/cascade-lake/2nd-gen-intel-xeon-scalable-processors.html ; and https://ark.intel.com/content/www/us/en/ark/products/97340/intel-c622-chipset.html

Chipset	Intel® C620 series (C622), supporting 10GbE

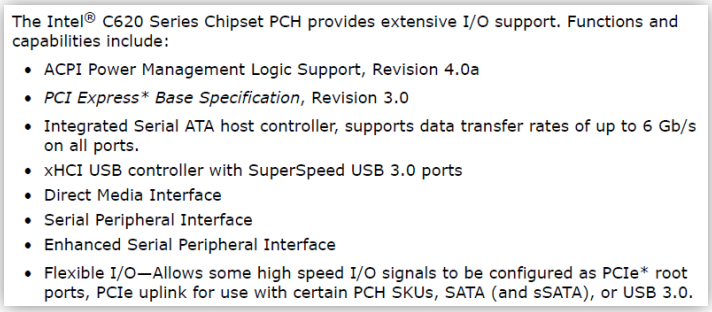
https://www.intel.com/content/www/us/en/design/products-and-solutions/processors-and-chipsets/cascade-lake/2nd-gen-intel-xeon-scalable-processors.html



https://www.intel.com/content/www/us/en/design/products-and-solutions/processors-and-chipsets/cascade-lake/2nd-gen-intel-xeon-scalable-processors.html

The Intel Xeon Processor Scalable Family is the next generation of 64-bit, multi-core server processor built on 14-nm process technology. The processor supports up to 46 bits of physical address space and 48 bits of virtual address space. The processor is designed for a platform consisting of at least one Intel Xeon Scalable Family processor and the Platform Controller Hub (PCH). Included in this family of processors are integrated memory controller (IMC) and an Integrated I/O (IIO) on a single silicon die.

Intel® Xeon® Processor Scalable Family Datasheet, Vol. 1, p. 7 (May 2018 Doc. No. 336062-003).

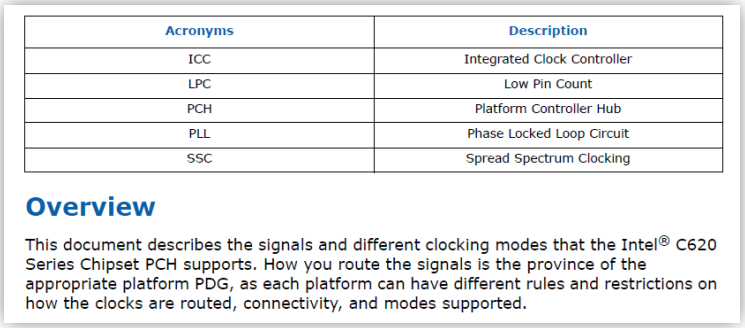


The Intel® C620 Series Chipset PCH provides extensive I/O support. Functions and capabilities include:

- ACPI Power Management Logic Support, Revision 4.0a
- *PCI Express* Base Specification*, Revision 3.0
- Integrated Serial ATA host controller, supports data transfer rates of up to 6 Gb/s on all ports.
- xHCI USB controller with SuperSpeed USB 3.0 ports
- Direct Media Interface
- Serial Peripheral Interface
- Enhanced Serial Peripheral Interface
- Flexible I/O—Allows some high speed I/O signals to be configured as PCIe* root ports, PCIe uplink for use with certain PCH SKUs, SATA (and sSATA), or USB 3.0.

Intel® C620 Series Chipset Platform Controller Hub Datasheet, p. 34, 38 (May 2019 Doc. No. 336067-007US)

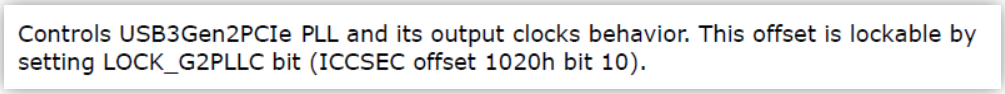
57. The Intel C621 PCH used in the K888G4 – Performance Server System has an Integrated Clock Controller (ICC) that includes PLL circuitry, which generates different clock frequencies to convey the PCI bus transactions and USB transactions through the PCIe and USB channels based on the different clock frequencies.



Acronyms	Description
ICC	Integrated Clock Controller
LPC	Low Pin Count
PCH	Platform Controller Hub
PLL	Phase Locked Loop Circuit
SSC	Spread Spectrum Clocking

Overview

This document describes the signals and different clocking modes that the Intel® C620 Series Chipset PCH supports. How you route the signals is the province of the appropriate platform PDG, as each platform can have different rules and restrictions on how the clocks are routed, connectivity, and modes supported.



Controls USB3Gen2PCIe PLL and its output clocks behavior. This offset is lockable by setting LOCK_G2PLLC bit (ICCSEC offset 1020h bit 10).

Intel® C620 Series Chipset Platform Controller Hub Datasheet, p. 98-116 (May 2019 Doc. No. 336067-007US).

58. The Intel processors used in the K888G4 – Performance Server System also have integrated clock circuitry that includes PLL circuitry, which generates different clock frequencies to convey the PCI bus transactions and USB transactions through the PCIe channels based on the different clock frequencies.

Clock multiplying within the processor is provided by the internal phase locked loop (PLL), which requires a constant frequency BCLK{0/1/2}_DP, BCLK{0/1/2}_DN input, with exceptions for spread spectrum clocking. DC specifications for the BCLK{0/1/2}_DP, BCLK{0/1/2}_DN inputs are provided in Section 2.8.3.7.

System Reference Clock (BCLK{0/1/2}) Signals

Signal Name	Description
BCLK{0,1,2}_DN/DP	Reference Clock Differential input. These pins provide the required reference inputs to various PLLs inside the processor, such as Intel UPI and PCIe. BCLK0, BCLK1 and BCLK2 run at 100 MHz from the same clock source.

Intel® Xeon® Processor Scalable Family Datasheet, Vol. 1, p. 15, 56 (May 2018 Doc. No. 336062-003)

8.6.2 100-MHz Differential Clocks

CLKOUT_NSSCCAP[1:0] are a pair of 100 MHz differential clocks that can have spread spectrum enabled and disabled on them independently of the rest of the 100 MHz differential clocks. This can be done because these clocks are sourced from a different PLL than the rest of the 100 MHz clocks. One effect of this is that these clocks can not be used to drive the BLCK inputs on the CPU, drive clock inputs to PCIe slots/devices that connect to the CPU, or clocks inputs to PCIe slots/devices that connect to the PCH. They are best considered independent clocks that can be used by components that do not need them to be used for transferring data between the CPUs and the PCHs. For example, if you had a SAS controller on the board that needed 100 MHz non-spread clocks for transferring data between the controller and the hard drives, the CLKOUT_NSSCCAP clocks could be used for this purpose.

The rest of the clocks (CLKOUT_ITPXDP, CLKOUT_PLAT[1:0], CLKOUT_SRC_N/P_[15:0]) are all generated by the same PLL, and operate the same with regards to spread spectrum. SSC is either on for all these clocks, or off. The PLL for these clocks also provides the clocking for USB3. The USB3 specification requires SSC to be turned on with a certain range, resulting in these clocks all, by default, having spread spectrum enabled operating in that mode. It is possible to disable SSC on these clocks, but that will end up in non-compliance with the USB3 specification.

While all are 100 MHz clocks, there are some differences between the clocks with regards to power and ground connections. For connections to the CPU BCLKs, CLKOUT_SRC clocks must be used. See the appropriate Platform Design Guide for more details on clock selection.

Intel® C620 Series Chipset Platform Controller Hub Datasheet, p. 102 (May 2019 Doc. No. 336067-007US)

59. P47G4 – Single-Socket HPC/AI/VDI Server is a modular computer system that can run on various server operating systems.

https://ebg.inventec.com/en/product/Server/2U/P47G4

60. The P47G4 – Single-Socket HPC/AI/VDI Server uses AMD® EPYC™ Processor Family processors, which have integrated interface controllers on a single chip to drive the PCIe channels connected to the processor.

Processor	Single Socket; AMD® EPYCTM Processor Family
Chipset	SoC, supporting 128 PCIe Gen3 lanes

https://ebg.inventec.com/en/product/Server/2U/P47G4

AMD Infinity Architecture is a hybrid multi-die architecture that is reaching new heights with AMD EPYC™ 7002 Series processors. AMD Infinity Architecture now decouples two streams: eight dies for the processor cores, and one I/O die that supports security and communication outside the processor. With the agility to deliver the leading-edge process technology for CPU cores while letting I/O circuitry develop at its own rate, new capabilities can be brought to market faster with EPYC™ because its die design is not monolithic. This has allowed EPYC™ to race to leadership in the market and continue to innovate in the future.

https://www.amd.com/en/processors/epyc-7002-series

The use of multiple dies and a fast fabric interconnect allows for a system-on-chip (SoC) design that eliminates the need for many external support chips and the I/O latencies they induce. This balanced system approach gives you an abundance of resources so that you can match workloads and resources and make the best use of capital. You'll find that 1- and 2-socket servers with AMD EPYC processors satisfy most of your workload needs, helping you increase density and reduce capital, power, and cooling expenses. You can also optimize your software licensing costs. Whether you need 8 cores per processor or 64, you'll get the same "all in" feature set–I/O, memory, memory bandwidth, and security capabilities–to accelerate workloads and help safeguard information.

https://www.amd.com/system/files/documents/LE-70001-SB-InfinityArchitecture.pdf

61. The P47G4 – Single-Socket HPC/AI/VDI Server includes a variety of connectors that can couple the CPU to a console, including without limitation a power supply.

Form Factor	2U1N rack mount with slide rail W x H x D: 436.9x 86.9x 736.6 mm (17.20x 3.42x 29.00 inch)
Power Supply	1600W Platinum (1+1 redundancy)

https://ebg.inventec.com/en/product/Server/2U/P47G4

62. The AMD processors employed in the P47G4 – Single-Socket HPC/AI/VDI Server connect directly to LVDS channels that convey data bits in a serial stream using unidirectional pairs of lanes transmitting data in opposite directions, including Intel's PCIe channels.

AMD EPYC™ is the first and only current x86-architecture server processor supporting PCIe 4.0[6]. PCIe 4.0 delivers double the I/O performance over PCIe 3.0. You can use 128 lanes of I/O to double the network bandwidth that ties together HPC clusters and satisfies voracious needs for east-west bandwidth. For other application needs and in virtualized environments, you can connect with higher speed to GPU accelerators, NVMe drives, and you can even use integrated disk controllers to access spinning disks without the typical bottleneck of a PCIe RAID controller.

https://www.amd.com/en/processors/epyc-7002-series

63. The AMD processors employed in the P47G4 – Single-Socket HPC/AI/VDI Server also directly connect to LVDS channels that convey USB data packets through pairs of unidirectional differential signal paths in opposite directions—USB 3.x ports for external cables.

Rear IO Ports

- 1x USB Port 3.0
- 1x VGA Port
- 1x management Port
- 1x Serial Port

https://ebg.inventec.com/en/product/Server/2U/P47G4

An On-die Server Control Hub makes EPYC a True SoC

Every server requires a control hub to handle the run-of-the-mill I/O interfaces found on almost all systems. "Why not incorporate a hub on the server die itself, rather than use a discrete chip?" AMD's engineers asked. Control hubs often consume five to eight watts, and in the discrete case much of that power just goes into inter-chip communications. The EPYC team put a Server Control Hub (SCH) on the "Zeppelin" die, and tied it into the Scalable Control Fabric, where it can observe the activity of all the chips and links in the system. It provides four USB 3.0 ports, two SMBus ports, platform clock generation, along with a few other goodies everyone notices only when they're absent. This simplifies the design of EPYC motherboards, and saves a few watts as well, as compared with competitive platforms that still require external control hubs.

https://www.amd.com/system/files/documents/The-Energy-Efficient-AMD-EPYC-Design.pdf

64. The P47G4 – Single-Socket HPC/AI/VDI Server has system memory directly coupled to the CPU.

Memory	16x DDR4 DIMM slot

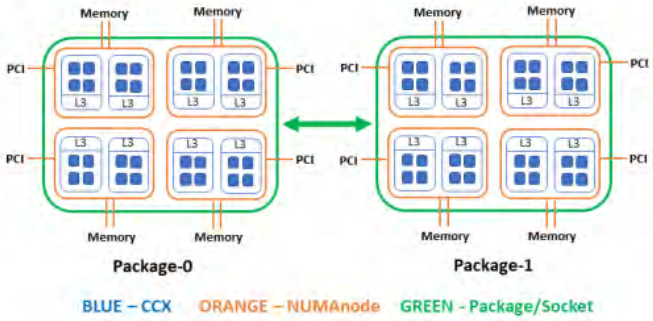
https://ebg.inventec.com/en/product/Server/2U/P47G4

EPYC 7002 series has 8 memory channels, supporting 3200 MHz DIMMs yielding 204.8 GB/s of bandwidth vs. the same class of Intel Scalable Gen 2 processors with only 6 memory channels and supporting 2933 MHz DIMMs yielding 140.8 GB/s of bandwidth. 204.8 / 140.8 = 1.454545 - 1.0 = .45 or 45% more. AMD EPYC has 45% more bandwidth. Class based on industry-standard pin-based (LGA) X86 processors. ROM-11

https://www.amd.com/system/files/documents/AMD-EPYC-7002-Series-Datasheet.pdf

6.1 CPU Layout

The following diagram shows a simplified schematic of a dual-socket AMD server.

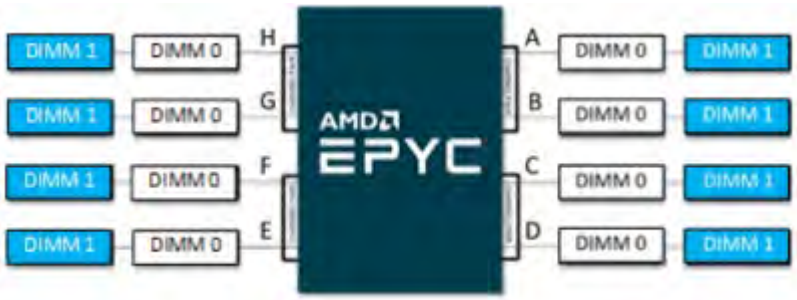


There is a rich hierarchy within the EPYC CPU which we explain here.

Each socket is comprised of 4 silicon dies (NUMA nodes, or 'Zeppelins') shown in orange. Eacl Zeppelin

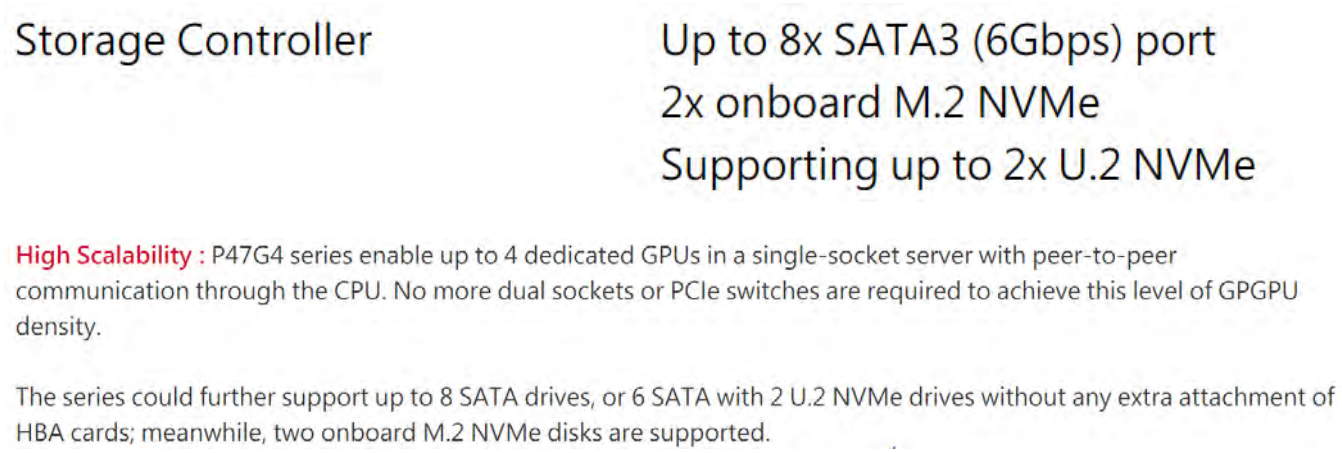
- provides 2 memory channels, i.e. 8 memory channels per socket
- provides PCIe gen3 slots (each OEM individually decides how to present/consume these resources)
- Is connected to the remaining 3 Zeppelins within the socket via the internal Global Memory Interconnect, or "Infinity Fabric". This enables each NUMA node to access the memory and PCI capabilities associated with its counterparts both within the socket and between sockets

http://developer.amd.com/wp-content/resources/56420.pdf



https://developer.amd.com/wp-content/resources/56502_1.00-PUB.pdf

65. The P47G4 – Single-Socket HPC/AI/VDI Server has a mass storage hard drive directly coupled to the CPU.



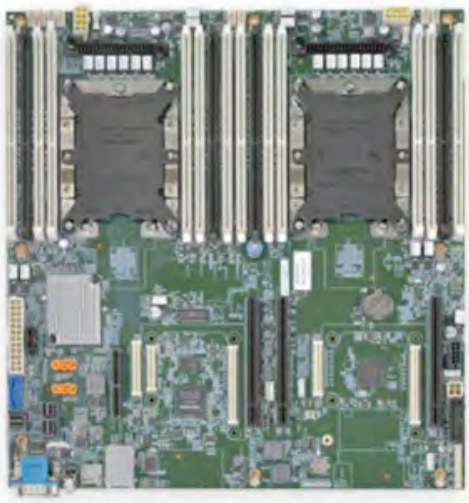
https://ebg.inventec.com/en/product/Server/2U/P47G4

66. The AMD® EPYC™ Processor Family processors used in the P47G4 – Single-Socket HPC/AI/VDI Server includes PLL circuitry, which generates different clock frequencies to convey the PCI bus transactions and USB transactions through the PCIe and USB channels based on the different clock frequencies. The AMD® EPYC™ Processor Family processors include multiple PLLS to facilitate granular frequency changes for CPU cores and I/O for better efficiency.

https://www.amd.com/system/files/documents/understanding-power-management.pdf

The Accused Motherboards

67. The B880G4 – Common EATX Motherboard is a printed circuit board.

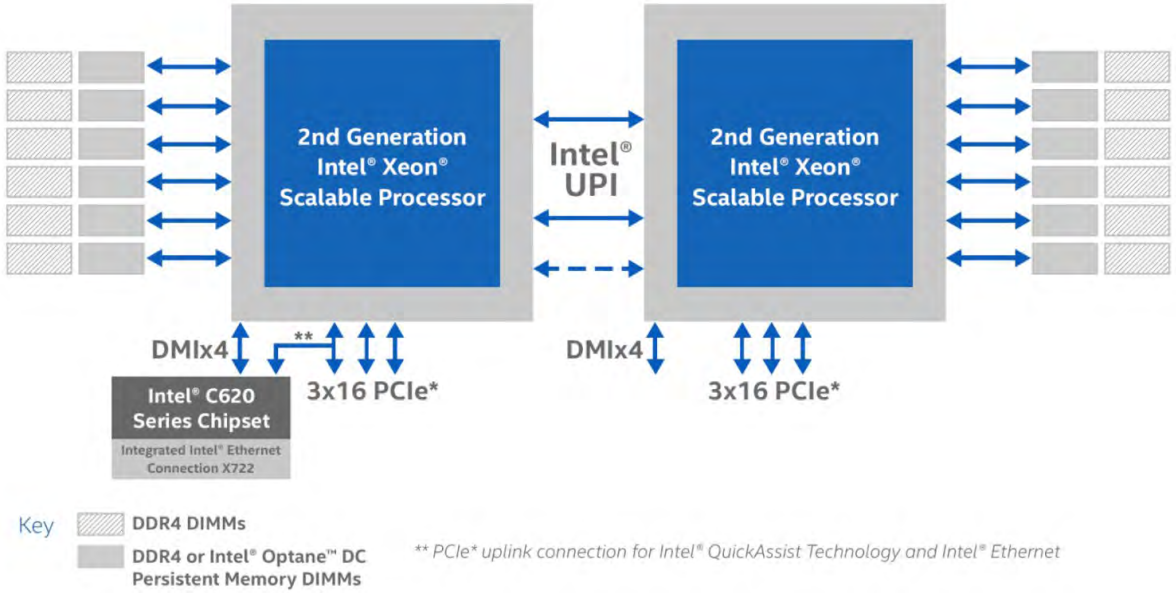


https://ebg.inventec.com/en/product/Motherboard/Intel/B880G4

68. The B880G4 – Common EATX Motherboard uses Intel® Xeon® Processor Scalable Family, which have integrated interface controllers on a single chip to drive the PCIe channels connected to the processor.

Processor	Dual Socket (LGA-3647); Intel® Xeon® Processor Scalable Family TDP: up to 205W

https://ebg.inventec.com/en/product/Motherboard/Intel/B880G4

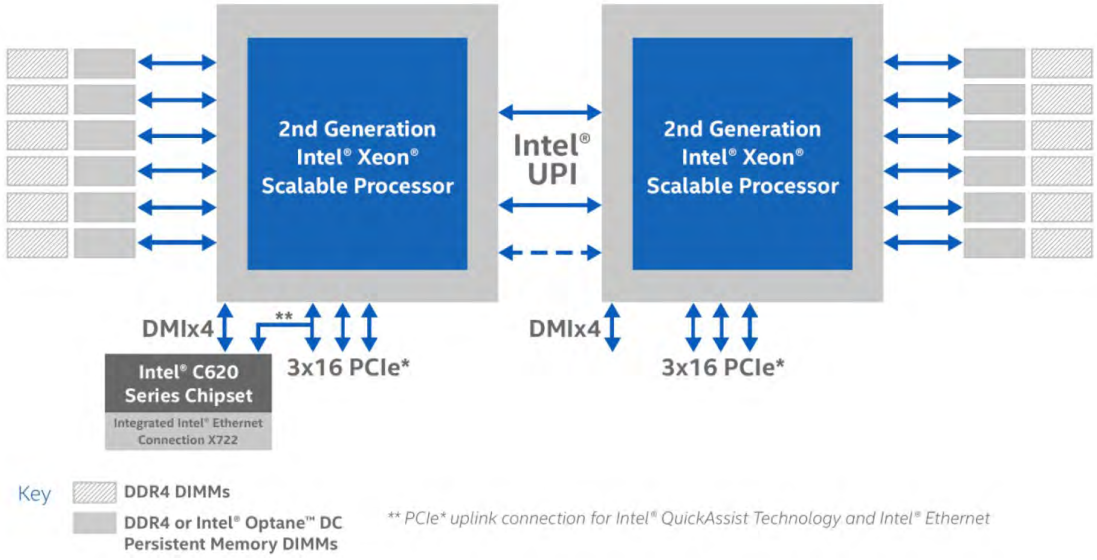


https://www.intel.com/content/www/us/en/design/products-and-solutions/processors-and-chipsets/cascade-lake/2nd-gen-intel-xeon-scalable-processors.html

69. The Intel® Xeon® Processor Scalable Family employed in the B880G4 – Common EATX Motherboard directly connect to LVDS channels that convey data bits in a serial stream using unidirectional pairs of lanes transmitting data in opposite direction, including Intel® Xeon® Processor Scalable Family's DMI and PCIe channels, thereby increasing data throughput. For example and without limitation, this includes a peripheral device such as the SATA SSDs.

High Scalability and IO Flexibility: B880G4 boasts high-level of IO flexibility that optimizes the scale-out fabrics, offering multiple storage options, which include two M.2 SATA SSDs from SATA connectors, or two M.2 NVMe via interposer connections, and a variety of storage mezzanine cards. Meanwhile, a variety of network choices are provided through the PCH PHY and up to two OCP 2.0 mezzanine slots, ranging from 10G Ethernet to 100G (optical or Base-T, compatible with OCP 2.0). Standard PCIe card option is supported too by the PCIe Gen3 x16 expansion slot. The high-speed performance and IO flexibility are realized by B880G4, catering to suitable demands of different application procedures.

https://ebg.inventec.com/en/product/Motherboard/Intel/B880G4



https://www.intel.com/content/www/us/en/design/products-and-solutions/processors-and-chipsets/cascade-lake/2nd-gen-intel-xeon-scalable-processors.html

70. The B880G4 – Common EATX Motherboard has socket for system memory and system memory directly coupled to the CPU.

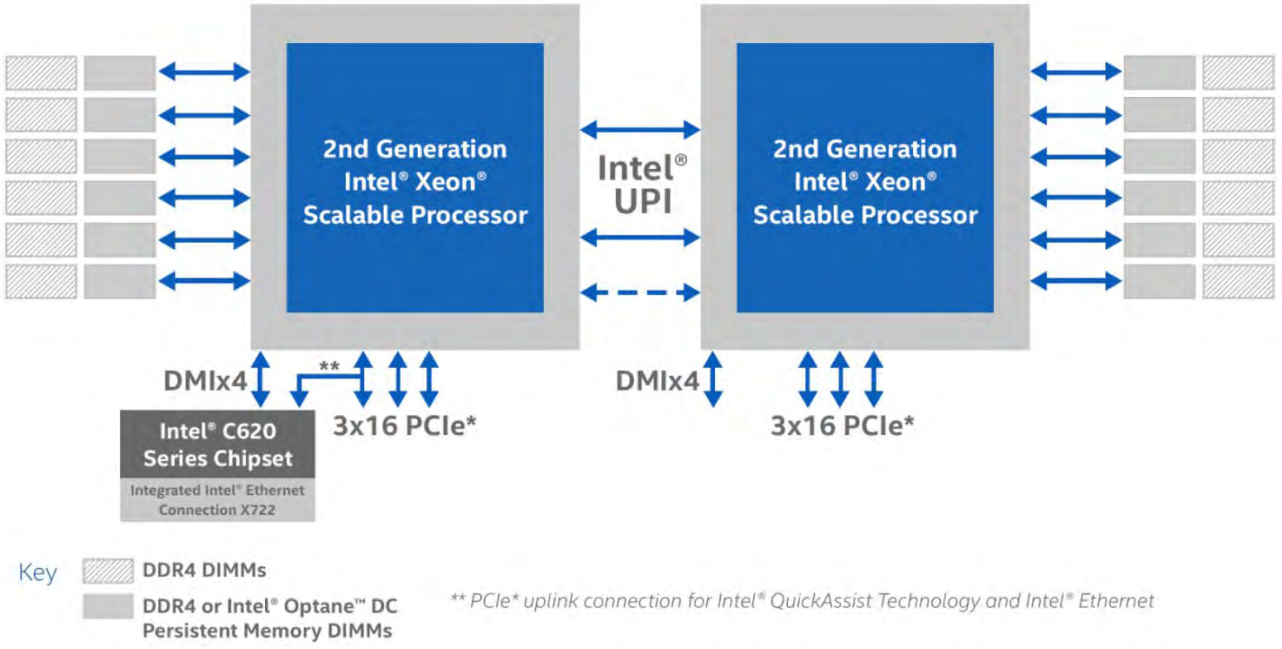
Memory Slot	16x DDR4 DIMM slot, 6 channels per socket with 2 DPC DIMM Type: ECC RDIMM, LRDIMM, 2667/1DPC, 2400/2DPC Supporting Intel® Optane™ Persistent Memory

https://ebg.inventec.com/en/product/Motherboard/Intel/B880G4

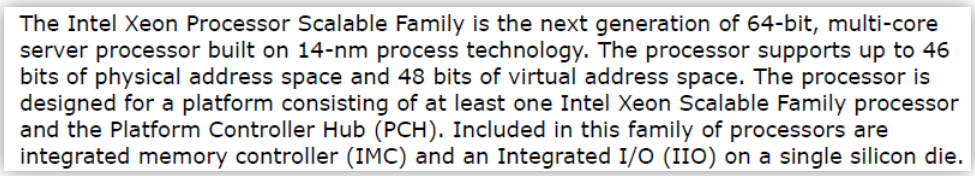
71. The Intel processors used in B880G4 – Common EATX Motherboard has a peripheral bridge called the C622 chipset PCH connected to the CPU via the DMI, which has an integrated interface controller. The C621 Chipset is part of the Intel C620 Series. *See* https://www.intel.com/content/www/us/en/design/products-and-solutions/processors-and-chipsets/cascade-lake/2nd-gen-intel-xeon-scalable-processors.html ; and https://ark.intel.com/content/www/us/en/ark/products/97340/intel-c622-chipset.html

Chipset	Intel® C620 series (C622)

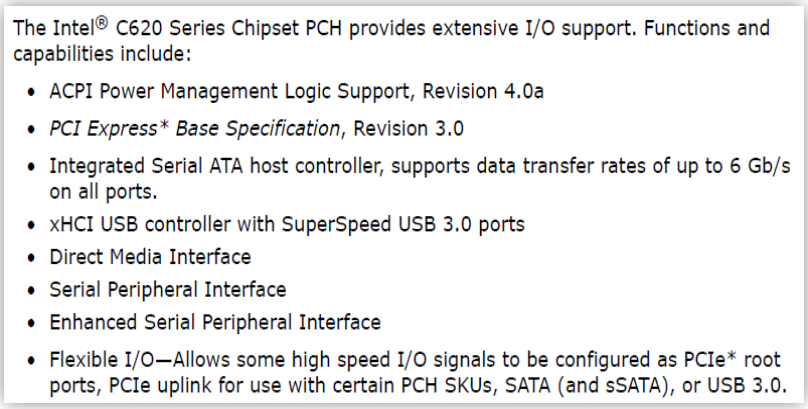
https://ebg.inventec.com/en/product/Motherboard/Intel/B880G4



https://www.intel.com/content/www/us/en/design/products-and-solutions/processors-and-chipsets/cascade-lake/2nd-gen-intel-xeon-scalable-processors.html


The Intel Xeon Processor Scalable Family is the next generation of 64-bit, multi-core server processor built on 14-nm process technology. The processor supports up to 46 bits of physical address space and 48 bits of virtual address space. The processor is designed for a platform consisting of at least one Intel Xeon Scalable Family processor and the Platform Controller Hub (PCH). Included in this family of processors are integrated memory controller (IMC) and an Integrated I/O (IIO) on a single silicon die.

Intel® Xeon® Processor Scalable Family Datasheet, Vol. 1, p. 7 (May 2018 Doc. No. 336062-003).


The Intel® C620 Series Chipset PCH provides extensive I/O support. Functions and capabilities include:

- ACPI Power Management Logic Support, Revision 4.0a
- *PCI Express* Base Specification*, Revision 3.0
- Integrated Serial ATA host controller, supports data transfer rates of up to 6 Gb/s on all ports.
- xHCI USB controller with SuperSpeed USB 3.0 ports
- Direct Media Interface
- Serial Peripheral Interface
- Enhanced Serial Peripheral Interface
- Flexible I/O—Allows some high speed I/O signals to be configured as PCIe* root ports, PCIe uplink for use with certain PCH SKUs, SATA (and sSATA), or USB 3.0.

Intel® C620 Series Chipset Platform Controller Hub Datasheet, p. 34, 38 (May 2019 Doc. No. 336067-007US).

72. The Intel C621 PCH used in the B880G4 – Common EATX Motherboard has an Integrated Clock Controller (ICC) that includes PLL circuitry, which generates different clock frequencies to convey the PCI bus transactions and USB transactions through the PCIe and USB channels based on the different clock frequencies.

Acronyms	Description
ICC	Integrated Clock Controller
LPC	Low Pin Count
PCH	Platform Controller Hub
PLL	Phase Locked Loop Circuit
SSC	Spread Spectrum Clocking

Overview

This document describes the signals and different clocking modes that the Intel® C620 Series Chipset PCH supports. How you route the signals is the province of the appropriate platform PDG, as each platform can have different rules and restrictions on how the clocks are routed, connectivity, and modes supported.

Controls USB3Gen2PCIe PLL and its output clocks behavior. This offset is lockable by setting LOCK_G2PLLC bit (ICCSEC offset 1020h bit 10).

8.6.2 100-MHz Differential Clocks

CLKOUT_NSSCCAP[1:0] are a pair of 100 MHz differential clocks that can have spread spectrum enabled and disabled on them independently of the rest of the 100 MHz differential clocks. This can be done because these clocks are sourced from a different PLL than the rest of the 100 MHz clocks. One effect of this is that these clocks can not be used to drive the BLCK inputs on the CPU, drive clock inputs to PCIe slots/devices that connect to the CPU, or clocks inputs to PCIe slots/devices that connect to the PCH. They are best considered independent clocks that can be used by components that do not need them to be used for transferring data between the CPUs and the PCHs. For example, if you had a SAS controller on the board that needed 100 MHz non-spread clocks for transferring data between the controller and the hard drives, the CLKOUT_NSSCCAP clocks could be used for this purpose.

The rest of the clocks (CLKOUT_ITPXDP, CLKOUT_PLAT[1:0], CLKOUT_SRC_N/P_[15:0]) are all generated by the same PLL, and operate the same with regards to spread spectrum. SSC is either on for all these clocks, or off. The PLL for these clocks also provides the clocking for USB3. The USB3 specification requires SSC to be turned on with a certain range, resulting in these clocks all, by default, having spread spectrum enabled operating in that mode. It is possible to disable SSC on these clocks, but that will end up in non-compliance with the USB3 specification.

While all are 100 MHz clocks, there are some differences between the clocks with regards to power and ground connections. For connections to the CPU BCLKs, CLKOUT_SRC clocks must be used. See the appropriate Platform Design Guide for more details on clock selection.

Intel® C620 Series Chipset Platform Controller Hub Datasheet, p. 98-116 (May 2019 Doc. No. 336067-007US)

73. The Intel Xeon Scalable processor used in B880G4 – Common EATX Motherboard also has integrated clock circuitry that includes PLL circuitry, which generates different clock

frequencies to convey the PCI bus transactions and USB transactions through the PCIe channels based on the different clock frequencies.

Clock multiplying within the processor is provided by the internal phase locked loop (PLL), which requires a constant frequency BCLK{0/1/2}_DP, BCLK{0/1/2}_DN input, with exceptions for spread spectrum clocking. DC specifications for the BCLK{0/1/2}_DP, BCLK{0/1/2}_DN inputs are provided in Section 2.8.3.7.

System Reference Clock (BCLK{0/1/2}) Signals

Signal Name	Description
BCLK{0,1,2}_DN/DP	Reference Clock Differential input. These pins provide the required reference inputs to various PLLs inside the processor, such as Intel UPI and PCIe. BCLK0, BCLK1 and BCLK2 run at 100 MHz from the same clock source.

Intel® Xeon® Processor Scalable Family Datasheet, Vol. 1, p. 15, 56 (May 2018 Doc. No. 336062-003)

74. The B880G4 – Common EATX Motherboard comprises a network controller coupled to the central processing unit.

Network Controller	**Onboard:** Dual 10G SFP+ **Supporting 25GE / 50GbE / 100GbE Mezz card**

https://ebg.inventec.com/en/product/Motherboard/Intel/B880G4

Inventec's Infringement

75. In view of the foregoing facts concerning the technical features and functionalities of the Accused Servers and Accused Motherboards (*see* ¶¶ 40-74), and on information and belief, when Inventec manufactures the Accused Servers and Accused Motherboards with peripheral bridges, it necessarily improves the speed and performance of the peripheral data communication in its computer products by using a method of manufacturing that includes the following steps: (a) connecting a CPU directly to a peripheral bridge on a printed circuit board; (b) directly connecting to the peripheral bridge one or more LVDS channels with pairs of unidirectional lanes that convey data in serial bit

streams in opposite directions; and (c) providing a connector with an LVDS channel to facilitate data communication with external peripherals using two unidirectional serial lanes to transmit data in opposite directions, including USB protocol data.

76. On information and belief, Inventec performs the foregoing manufacturing steps outside the United States to make the Accused Servers and then imports the Accused Servers into the United States to be marketed and sold.

77. Through making, using, selling, offering for sale, and importing the Accused Servers and Accused Motherboards with the features and functionalities alleged above, Inventec has and continues to infringe one or more of the claims in each of the ACQIS Patents.

78. Inventec's infringing conduct has caused injury and damage to ACQIS and ACQIS' licensees, and will continue to cause additional severe and irreparable injury and damage to ACQIS and ACQIS' licensees unless enjoined by this Court.

ACQIS Provided Inventec Actual Notice of its Infringement

79. On or around May 14, 2018, ACQIS notified Inventec, pursuant to 35 U.S.C. § 287(a), of all of the ACQIS Patents and Inventec's infringement thereof based on the Accused Servers and Accused Motherboards. Specifically, ACQIS' letter identified all of the ACQIS Patents asserted herein and described the applicability of the ACQIS Patents to the PCI Express, USB 3.0, and other computer interface technologies. ACQIS's letter specifically identified Inventec's various servers and related accessories, including the Accused Servers and Accused Motherboards addressed herein as using ACQIS' patented technologies. ACQIS also described the enforcement history of ACQIS's patent portfolio, and specifically noted a prior lawsuit enforcing ACQIS patents related to the presently-asserted ACQIS Patents, which resulted in a significant jury verdict against IBM.

80. ACQIS invited Inventec to discuss potential licensing arrangements to allow Inventec to continue to utilize the patented technologies in the ACQIS patent portfolio, including the ACQIS Patents.

81. Inventec responded and claimed that it does not infringe. Inventec continues to make, import, and sell the Accused Servers and Accused Motherboards identified in ACQIS's letter in willful violation of ACQIS' patent rights, or at the very least in reckless disregard of ACQIS' patent rights.

82. Upon receiving actual notice of the ACQIS Patents and how they apply to the Inventec's server products, Inventec chose to remain willfully blind to its own infringement and the infringement that it was inducing others to commit through the use of the Accused Servers and Accused Motherboards.

83. Inventec's choice continue making and selling the infringing Accused Servers and Accused Motherboards, is egregious and exceptional.

84. Inventec's conduct constitutes willful infringement of the ACQIS Patents, beginning at least as early as May 14, 2018.

Inventec's Indirect Infringement

85. Inventec indirectly infringes the ACQIS Patents under 35 U.S.C. § 271(b) by inducing third parties, such as importers, resellers, customers, and end users, to directly infringe the ACQIS Patents by using, offering for sale, selling and/or importing the Accused Servers in this District and elsewhere in the United States. For example, in the Inventec 2019 Annual Report, America is listed as a "Major Sales Territory" for the "Major Product Department" that includes "notebook computers, servers, and other electronic information products."

86. On information and belief, Inventec took affirmative acts to induce third parties to commit those direct infringing acts. Inventec did so by, at least actively promoting the Accused

Servers and Accused Motherboards for the U.S. market. For example, on information and belief, for the Accused Inventec Products sold in the United States, Inventec pursues and obtains approval from U.S. and state regulatory agencies to allow sales of such Inventec Products in the United States. Inventec competes for business in the United States. Inventec's website offers support for US consumers of the Accused Products and identifies US regional operation centers in the US, including in Silicon Valley and in Texas in both Austin and Houston. Inventec has taken these acts despite knowledge of the ACQIS Patents and the infringement by the Accused Servers and Accused Motherboards, Inventec knows and specifically intends that its customers will sell the infringing Accused Servers in the United States or cause the Accused Servers and Accused Motherboards to be sold in the United States.

87. Inventec's customers directly infringe the ACQIS Patents by importing the Accused Servers and Accused Motherboards into the United States, offering to sell and selling the Accused Servers in the United States, and using the Accused Servers in the United States.

88. Inventec further induces direct infringement of the ACQIS Patents by providing instruction and direction to end users of the Accused Servers about how to use the Accused Servers and Accused Motherboards in a manner that infringes one or more claims of the ACQIS Patents. Inventec knows and specifically intends that end users will use the Accused Servers and Accused Motherboards in an infringing manner as directed by Inventec. Inventec has configured the Accused Servers and Accused Motherboards in such a manner that direct infringing use necessarily occurs upon operation of the Accused Servers and Accused Motherboards in their normal, intended manner without any specific action of the end user other than turning on the product.

89. Inventec has induced others' direct infringement as stated above despite actual notice that the Accused Servers and Accused Motherboards infringe the ACQIS Patents, as set forth herein. Inventec therefore has caused its purchasers and end users to directly infringe the ACQIS Patents

with knowledge of the ACQIS Patents and with the specific intent, or at the very least willful blindness, that the purchasers and end users will directly infringe. Inventec knew the acts it induced (like importation, U.S. sales, and use by its customers) constituted infringement.

90. Inventec contributorily infringes the ACQIS Patents under 35 U.S.C. § 271(c). Inventec knew about the ACQIS Patents prior to this complaint. Inventec's products are especially made or especially adapted for use that results in an infringement of the ACQIS Patents. Inventec's products include features that are not staple articles of commerce suitable for substantial non-infringing uses. Inventec's products are a material part of the invention of the ACQIS Patents. Inventec's products are also sold, offered for sale, and used in configurations that do not have substantial non-infringing uses. The intended, normal use of Inventec's servers and motherboards results in infringement of the ACQIS Patents.

91. Inventec's acts of indirect infringement as stated herein have caused injury and damage to ACQIS, and will continue to cause additional severe and irreparable injury and damages to ACQIS in the future if not enjoined by this Court.

COUNT I
INFRINGEMENT OF U.S. PATENT NO. 9,529,768

92. ACQIS incorporates by this reference the allegations set forth in paragraphs 1 through 91 of this Complaint in support of its first cause of action as though fully set forth herein.

93. Pursuant to 35 U.S.C. § 282, the claims of the '768 patent are presumed valid.

94. In view of the foregoing facts and allegations, including paragraphs 13-39 and 40-74 above, Inventec has directly infringed and continues to directly infringe one or more claims of the '768 patent in violation of 35 U.S.C. § 271(a) by making, using, selling, offering to sell, and/or importing the Accused Servers.

95. Inventec's direct infringement of the '768 patent through its manufacture, use, offers to sell, sales, and importation of the Accused Servers is shown by way of the exemplary K888G4 – Performance Server System and P47G4 – Single-Socket HPC/AI/VDI Server servers as set forth in paragraphs 40-66 above, which demonstrates infringement of at least claim 13 of the '768 patent by showing:

(a) the K888G4 – Performance Server System and P47G4 – Single-Socket HPC/AI/VDI Server are computers;

(b) the K888G4 – Performance Server System and P47G4 – Single-Socket HPC/AI/VDI Server have central processing units (CPU) with integrated interface controllers in a single chip;

(c) the K888G4 – Performance Server System and P47G4 – Single-Socket HPC/AI/VDI Server computers have a first Low Voltage Differential Signal (LVDS) channel directly extending from the interface controller to convey address and data bits of a Peripheral Component Interconnect (PCI) bus transaction in a serial bit stream, wherein the first LVDS channel comprises first unidirectional, multiple, differential signal pairs to convey data in a first direction and second unidirectional, multiple, differential signal pairs to convey data in a second, opposite direction; and

(d) the K888G4 – Performance Server System and P47G4 – Single-Socket HPC/AI/VDI Server have system memory directly coupled to the CPU and interface controller.

96. ACQIS' infringement allegations against the Accused Servers are not limited to claim 13 of the '768 patent, and additional infringed claims will be identified through infringement contentions and discovery.

97. Inventec's direct infringement of the '768 patent through its manufacture, use, offers to sell, sales, and importation of the Accused Motherboards is shown by way of the exemplary

B880G4 – Common EATX Motherboard motherboards as set forth in paragraphs 67-74 above, which demonstrates infringement of at least claim 10 of the ’768 patent by showing:

(a) The B880G4 – Common EATX Motherboard is a printed circuit board;

(b) The B880G4 – Common EATX Motherboard comprises a central processing unit;

(c) The B880G4 – Common EATX Motherboard comprises a peripheral bridge directly coupled to the central processing unit without any intervening Peripheral Component Interconnect (PCI) bus;

(d) The B880G4 – Common EATX Motherboard comprises a low voltage differential signal (LVDS) channel directly extending from the peripheral bridge comprising two unidirectional, serial channels of multiple differential signal line pairs to convey data in opposite directions, wherein the LVDS channel conveys address and data bits of a PCI bus transaction in serial form; and

(e) The B880G4 – Common EATX Motherboard comprises a network controller coupled to the central processing unit.

98. ACQIS’ infringement allegations against the Accused Motherboards are not limited to claim 10 of the’768 patent, and additional infringed claims will be identified through infringement contentions and discovery.

99. As early as around May 14, 2018, and at least as of the filing of this Complaint, Inventec had actual notice of the ’768 patent and the infringement alleged herein.

100. Inventec’s actions as alleged herein, including those alleged in paragraphs 40-74, constitute induced infringement of at least claims 10 and 13 of the ’768 patent pursuant to 35 U.S.C. § 271(b).

101. Inventec's actions as alleged herein, including those alleged in paragraphs 40-74, constitute contributory infringement of at least claims 10 and 13 of the '768 patent under 35 U.S.C. § 271(c).

102. The above-described acts of direct and induced infringement committed by Inventec have caused injury and damage to ACQIS, and will continue to cause damages and irreparable harm to ACQIS unless enjoined.

103. ACQIS is entitled to recover all damages sustained as a result of Inventec's wrongful acts of infringement, but in no event less than a reasonable royalty pursuant to 35 U.S.C. § 284.

104. Inventec's infringement as described herein has been and continues to be willful and exceptional. Accordingly, ACQIS is entitled to recover enhanced damages up to three times the amount found or assessed at trial pursuant to 35 U.S.C. § 284, as well as its attorneys' fees pursuant to 35 U.S.C. § 285.

COUNT II
INFRINGEMENT OF U.S. PATENT NO. 9,703,750

105. ACQIS incorporates by this reference the allegations set forth in paragraphs 1 through 104 of this Complaint in support of its second cause of action as though fully set forth herein.

106. Pursuant to 35 U.S.C. § 282, the claims of the '750 patent are presumed valid.

107. In view of the foregoing facts and allegations, including paragraphs 13-39 and 40-74 above, Inventec has directly infringed and continues to directly infringe one or more claims of the '750 patent in violation of 35 U.S.C. § 271(a) by making, using, selling, offering to sell, and/or importing the Accused Servers.

108. Inventec's direct infringement of the '750 patent through its manufacture, use, offers to sell, sales, and importation of the Accused Servers is shown by way of the exemplary K888G4 – Performance Server System and P47G4 – Single-Socket HPC/AI/VDI Server servers as set forth in

paragraphs 40-66 above, which demonstrates infringement of at least claim 4 of the ’750 patent by showing:

(a) the K888G4 – Performance Server System and P47G4 – Single-Socket HPC/AI/VDI Server are computers;

(b) the K888G4 – Performance Server System and P47G4 – Single-Socket HPC/AI/VDI Server have central processing units (CPU) with integrated interface controllers in a single chip;

(c) the K888G4 – Performance Server System and P47G4 – Single-Socket HPC/AI/VDI Server have a first Low Voltage Differential Signal (LVDS) channel directly extending from the interface controller to convey address bits, data bits, and byte enable information bits of a Peripheral Component Interconnect (PCI) bus transaction in a serial bit stream, wherein the first LVDS channel comprises a first unidirectional, differential signal pair to convey data in a first direction and a second unidirectional, differential signal pair to convey data in a second, opposite direction;

(d) the K888G4 – Performance Server System and P47G4 – Single-Socket HPC/AI/VDI Server have system memory directly coupled to the integrated central processing unit and interface controller;

(e) the interface controller of the K888G4 – Performance Server System and P47G4 – Single-Socket HPC/AI/VDI Server comprises Phase-Locked Loop (PLL) clock circuitry capable of generating different clock frequencies;

(f) the interface controller of the K888G4 – Performance Server System and P47G4 – Single-Socket HPC/AI/VDI Server configures the first LVDS channel to convey the PCI bus transaction at different data transfer rates based on the different clock frequencies generated by the PLL clock circuitry; and

(g) and the interface controller of the K888G4 – Performance Server System and P47G4 – Single-Socket HPC/AI/VDI Server comprises a connector adapted to convey a serial bit stream of Universal Serial Bus (USB) protocol data packets in a second Low Voltage Differential Signal (LVDS) channel comprising two unidirectional, differential signal pairs that transmit data in opposite directions.

109. ACQIS' infringement allegations against the Accused Servers are not limited to claim 4 of the '750 patent, and additional infringed claims will be identified through infringement contentions and discovery.

110. Inventec's direct infringement of the '750 patent through its manufacture, use, offers to sell, sales, and importation of the Accused Motherboards is shown by way of the exemplary B880G4 – Common EATX Motherboard motherboards as set forth in paragraphs 67-74 above, which demonstrates infringement of at least claim 25 of the '750 patent by showing:

(a) The B880G4 – Common EATX Motherboard is a printed circuit board;

(b) The B880G4 – Common EATX Motherboard comprises an integrated central processing unit and interface controller in a single chip;

(c) The B880G4 – Common EATX Motherboard comprises a Low Voltage Differential Signal (LVDS) channel directly extending from the integrated central processing unit and interface controller to convey address bits, data bits, and byte enable information bits of a Peripheral Component Interconnect (PCI) bus transaction in a serial form, wherein the LVDS channel comprises first unidirectional, multiple, differential signal line pairs to convey data in a first direction and second unidirectional, multiple, differential signal line pairs to convey data in a second, opposite direction; and

(d) The B880G4 – Common EATX Motherboard comprises a socket for a system memory module directly coupled to the integrated central processing unit and interface controller.

111. ACQIS' infringement allegations against the Accused Motherboards are not limited to claim 25 of the '750 patent, and additional infringed claims will be identified through infringement contentions and discovery.

112. As early as around May 14, 2018, and at least as of the filing of this Complaint, Inventec had actual notice of the '750 patent and the infringement alleged herein.

113. Inventec's actions as alleged herein, including those alleged in paragraphs 40-74, constitute induced infringement of at least claims 4 and 25 of the '750 patent pursuant to 35 U.S.C. § 271(b).

114. Inventec's actions as alleged herein, including those alleged in paragraphs 40-74, constitute contributory infringement of at least claims 4 and 25 of the '750 patent under 35 U.S.C. § 271(c).

115. The above-described acts of direct and induced infringement committed by Inventec have caused injury and damage to ACQIS, and will continue to cause damages and irreparable harm to ACQIS unless enjoined.

116. ACQIS is entitled to recover all damages sustained as a result of Inventec's wrongful acts of infringement, but in no event less than a reasonable royalty pursuant to 35 U.S.C. § 284.

117. Inventec's infringement as described herein has been and continues to be willful and exceptional. Accordingly, ACQIS is entitled to recover enhanced damages up to three times the amount found or assessed at trial pursuant to 35 U.S.C. § 284, as well as its attorneys' fees pursuant to 35 U.S.C. § 285.

COUNT III
INFRINGEMENT OF U.S. PATENT NO. 8,977,797

118. ACQIS incorporates by this reference the allegations set forth in paragraphs 1 through 117 of this Complaint in support of its third cause of action as though fully set forth herein.

119. Pursuant to 35 U.S.C. § 282, the claims of the ’797 patent are presumed valid.

120. In view of the foregoing facts and allegations, including paragraphs 13-39 and 40-74 above, Inventec has directly infringed and continues to directly infringe one or more claims of the ’797 patent in violation of 35 U.S.C. § 271(g) by using one or more of the methods claimed in the ’797 patent to manufacture the Accused Servers and then importing, selling, offering to sell, and/or using the Accused Servers in the United States.

121. The Accused Servers made using the methods claimed in the ’797 patent are not trivial or nonessential components of other products and are not materially changed by subsequent processes.

122. Inventec’s direct infringement of the ’797 patent through its manufacture, use, offers to sell, sales, and importation of the Accused Servers is shown by way of the exemplary K888G4 – Performance Server System as set forth in paragraphs 40-58 above, which demonstrate that to manufacture the K888G4 – Performance Server System, Inventec performs the following actions, which results in direct infringement of at least claim 7 of the ’797 patent upon importation and/or sale of the K888G4 – Performance Server System in the United States:

(a) Inventec improves the storage data throughput of the K888G4 – Performance Server System, which is a computer;

(b) Inventec connects a Central Processing Unit (CPU) directly to a peripheral bridge on a printed circuit board of the K888G4 – Performance Server System;

(c) Inventec connects a Low Voltage Differential Signal (LVDS) channel directly to the peripheral bridge on the printed circuit board of the K888G4 – Performance Server System, the LVDS channel comprising two unidirectional, serial channels that transmit data in opposite directions;

(d) Inventec increases data throughput of the serial channels in the K888G4 – Performance Server System by providing each channel with multiple pairs of differential signal lines;

(e) Inventec conveys encoded address and data bits of a Peripheral Component Interconnect (PCI) bus transaction in serial form over the serial channels of the K888G4 – Performance Server System to preserve the PCI bus transaction;

(f) Inventec couples the peripheral bridge of the K888G4 – Performance Server System to a mass storage device through the LVDS channel; and

(g) Inventec applies power to the computer system of the K888G4 – Performance Server System.

123. ACQIS' infringement allegations against the Accused Servers are not limited to claim 7 of the '797 patent, and additional infringed claims will be identified through infringement contentions and discovery.

124. Inventec's direct infringement of the '797 patent through its manufacture, use, offers to sell, sales, and importation of the Accused Motherboards is shown by way of the exemplary B880G4 – Common EATX Motherboard motherboards as set forth in paragraphs 67-74 above, which demonstrates infringement of at least claim 14 of the '797 patent by showing:

(a) Inventec improves the data throughput on the B880G4 – Common EATX Motherboard, which is a motherboard;

(b) Inventec mounts a Central Processing Unit (CPU) on the B880G4 – Common EATX Motherboard;

(c) Inventec connects a Low Voltage Differential Signal (LVDS) channel directly to the CPU on the B880G4 – Common EATX Motherboard, the LVDS channel comprising two unidirectional, serial channels that transmit data in opposite directions;

(d) Inventec increases the data throughput of the serial channels of the B880G4 – Common EATX Motherboard by providing each channel with multiple pairs of differential signal lines;

(e) Inventec conveys encoded address and data bits of a Peripheral Component Interconnect (PCI) bus transaction in serial form over the serial channels of the B880G4 – Common EATX Motherboard to preserve the PCI bus transaction; and

(f) Inventec couples the CPU to a peripheral device attached to the B880G4 – Common EATX Motherboard through the LVDS channel.

125. ACQIS' infringement allegations against the Accused Motherboards are not limited to claim 14 of the'797 patent, and additional infringed claims will be identified through infringement contentions and discovery.

126. As early as around May 14, 2018, and at least as of the filing of this Complaint, Inventec had actual notice of the '797 patent and the infringement alleged herein.

127. Inventec's actions as alleged herein, including those alleged in paragraphs 40-74, constitute induced infringement of at least claims 7 and 14 of the '797 patent pursuant to 35 U.S.C. § 271(b).

128. Inventec's actions as alleged herein, including those alleged in paragraphs 40-74, constitute contributory infringement of at least claims 7 and 14 of the'797 patent under 35 U.S.C. § 271(c).

129. The above-described acts of direct and induced infringement committed by Inventec have caused injury and damage to ACQIS, and will continue to cause damages and irreparable harm to ACQIS unless enjoined.

130. ACQIS is entitled to recover all damages sustained as a result of Inventec's wrongful acts of infringement, but in no event less than a reasonable royalty pursuant to 35 U.S.C. § 284.

131. Inventec's infringement as described herein has been and continues to be willful and exceptional. Accordingly, ACQIS is entitled to recover enhanced damages up to three times the amount found or assessed at trial pursuant to 35 U.S.C. § 284, as well as its attorneys' fees pursuant to 35 U.S.C. § 285.

COUNT IV
INFRINGEMENT OF U.S. PATENT NO. 8,756,359

132. ACQIS incorporates by this reference the allegations set forth in paragraphs 1 through 131 of this Complaint in support of its fourth cause of action as though fully set forth herein.

133. Pursuant to 35 U.S.C. § 282, the claims of the '359 patent are presumed valid.

134. In view of the foregoing facts and allegations, including paragraphs 13-39 and 40-66 above, Inventec has directly infringed and continues to directly infringe one or more claims of the '359 patent in violation of 35 U.S.C. § 271(a) by making, using, selling, offering to sell, and/or importing the Accused Servers.

135. Inventec's direct infringement of the '359 patent through its manufacture, use, offers to sell, sales, and importation of the Accused Servers is shown by way of the exemplary K888G4 – Performance Server System and P47G4 – Single-Socket HPC/AI/VDI Server servers as set forth in paragraphs 40-66 above, which demonstrates infringement of at least claim 6 of the '359 patent by showing:

(a) the K888G4 – Performance Server System and P47G4 – Single-Socket HPC/AI/VDI Server are computers;

(b) the K888G4 – Performance Server System and P47G4 – Single-Socket HPC/AI/VDI Server have a connector that is configured to couple to a console;

(c) the K888G4 – Performance Server System and P47G4 – Single-Socket HPC/AI/VDI Server have a central processing unit;

(d) the K888G4 – Performance Server System and P47G4 – Single-Socket HPC/AI/VDI Server have a first Low Voltage Differential Signal (LVDS) channel directly extending from the central processing unit, comprising a first unidirectional, differential signal line pair to convey data in a first direction and a second unidirectional, differential signal line pair to convey data in a second, opposite direction; and

(e) the K888G4 – Performance Server System and P47G4 – Single-Socket HPC/AI/VDI Server have a second LVDS channel that can couple to the console through the connector, comprising two unidirectional, differential signal line pairs to convey data in opposite directions, wherein the second LVDS channel is adapted to transmit data packets in accordance with a Universal Serial Bus (USB) protocol.

136. ACQIS' infringement allegations against the Accused Servers are not limited to claim 6 of the '359 patent, and additional infringed claims will be identified through infringement contentions and discovery.

137. As early as around May 14, 2018, and at least as of the filing of this Complaint, Inventec had actual notice of the '359 patent and the infringement alleged herein.

138. Inventec's actions as alleged herein, including those alleged in paragraphs 40-66, constitute induced infringement of at least claim 6 of the '359 patent pursuant to 35 U.S.C. § 271(b).

139. Inventec's actions as alleged herein, including those alleged in paragraphs 40-66, constitute contributory infringement of at least claim 6 of the '359 patent under 35 U.S.C. § 271(c).

140. The above-described acts of direct and induced infringement committed by Inventec have caused injury and damage to ACQIS, and will continue to cause damages and irreparable harm to ACQIS unless enjoined.

141. ACQIS is entitled to recover all damages sustained as a result of Inventec's wrongful acts of infringement, but in no event less than a reasonable royalty pursuant to 35 U.S.C. § 284.

142. Inventec's infringement as described herein has been and continues to be willful and exceptional. Accordingly, ACQIS is entitled to recover enhanced damages up to three times the amount found or assessed at trial pursuant to 35 U.S.C. § 284, as well as its attorneys' fees pursuant to 35 U.S.C. § 285.

COUNT V
INFRINGEMENT OF RE44,654

143. ACQIS incorporates by this reference the allegations set forth in paragraphs 1 through 142 of this Complaint in support of its fifth cause of action as though fully set forth herein.

144. Pursuant to 35 U.S.C. § 282, the claims of the '654 patent are presumed valid.

145. In view of the foregoing facts and allegations, including paragraphs 13-39 and 40-66 above, Inventec has directly infringed and continues to directly infringe one or more claims of the '654 patent in violation of 35 U.S.C. § 271(a) by making, using, selling, offering to sell, and/or importing the Accused Servers.

146. Inventec's direct infringement of the '654 patent through its manufacture, use, offers to sell, sales, and importation of the Accused Servers is shown by way of the exemplary K888G4 – Performance Server System as set forth in paragraphs 40-66 above, which demonstrates infringement of at least claim 14 of the '654 patent by showing:

(a) Inventec increases external peripheral data communication speed of the K888G4 – Performance Server System, which is a computer;

(b) Inventec connects a Central Processing Unit (CPU) directly to a peripheral bridge on a printed circuit board of the K888G4 – Performance Server System;

(c) Inventec connects a first Low Voltage Differential Signal (LVDS) channel directly to the peripheral bridge on the printed circuit board, the first LVDS channel comprising two unidirectional, serial channels that transmit data in opposite directions to the K888G4 –

Performance Server System;

(d) Inventec provides a connector for the K888G4 – Performance Server System for connection to a console;

(e) Inventec provides a second LVDS channel to couple to the console through the connector, the second LVDS channel comprising two unidirectional, serial channels that transmit data in opposite directions;

(f) Inventec conveys encoded address and data bits of a Peripheral Component Interconnect (PCI) bus transaction on the K888G4 – Performance Server System in serial form over the first LVDS channel and the second LVDS channel to preserve the PCI bus transaction; and

(g) Inventec enables the PCI bus transaction on the K888G4 – Performance Server System to be conveyed serially through the second LVDS channel to the console to improve peripheral data communication speed between the computer and the console.

147. ACQIS' infringement allegations against the Accused Servers are not limited to claim 14 of the '654 patent, and additional infringed claims will be identified through infringement contentions and discovery.

148. As early as around May 14, 2018, and at least as of the filing of this Complaint, Inventec had actual notice of the '654 patent and the infringement alleged herein.

149. Inventec's actions as alleged herein, including those alleged in paragraphs 40-66, constitute induced infringement of at least claim 14 of the '654 patent pursuant to 35 U.S.C. § 271(b).

150. Inventec's actions as alleged herein, including those alleged in paragraphs 40-66, constitute contributory infringement of at least claim 14 of the'654 patent under 35 U.S.C. § 271(c).

151. The above-described acts of direct and induced infringement committed by Inventec have caused injury and damage to ACQIS, and will continue to cause damages and irreparable harm to ACQIS unless enjoined.

152. ACQIS is entitled to recover all damages sustained as a result of Inventec's wrongful acts of infringement, but in no event less than a reasonable royalty pursuant to 35 U.S.C. § 284.

153. Inventec's infringement as described herein has been and continues to be willful and exceptional. Accordingly, ACQIS is entitled to recover enhanced damages up to three times the amount found or assessed at trial pursuant to 35 U.S.C. § 284, as well as its attorneys' fees pursuant to 35 U.S.C. § 285.

COUNT VI
INFRINGEMENT OF RE44,739

154. ACQIS incorporates by this reference the allegations set forth in paragraphs 1 through 153 of this Complaint in support of its sixth cause of action as though fully set forth herein.

155. Pursuant to 35 U.S.C. § 282, the claims of the '739 patent are presumed valid.

156. In view of the foregoing facts and allegations, including paragraphs 13-39 and 40-66 above, Inventec has directly infringed and continues to directly infringe one or more claims of the '739 patent in violation of 35 U.S.C. § 271(a) by making, using, selling, offering to sell, and/or importing the Accused Servers.

157. Inventec's direct infringement of the '739 patent through its manufacture, use, offers to sell, sales, and importation of the Accused Servers is shown by way of the exemplary P47G4 – Single-Socket HPC/AI/VDI Server as set forth in paragraphs 40-66 above, which demonstrates infringement of at least claim 14 of the '739 patent by showing:

(a) the P47G4 – Single-Socket HPC/AI/VDI Server are computers;

(b) the P47G4 – Single-Socket HPC/AI/VDI Server have a central processing unit directly connected to a first Low Voltage Differential Signal (LVDS) channel comprising two unidirectional, differential signal pairs to transmit Universal Serial Bus (USB) Protocol data in opposite directions;

(c) the P47G4 – Single-Socket HPC/AI/VDI Server main memory directly connected to the central processing unit;

(d) the P47G4 – Single-Socket HPC/AI/VDI Server have connector to couple to an external cable; and

(e) the P47G4 – Single-Socket HPC/AI/VDI Server have a second LVDS channel comprising two unidirectional, differential signal pairs to transmit data in opposite directions, wherein the second LVDS channel couples to the connector.

158. ACQIS' infringement allegations against the Accused Servers are not limited to claim 14 of the '739 patent, and additional infringed claims will be identified through infringement contentions and discovery.

159. As early as around May 14, 2018, and at least as of the filing of this Complaint, Inventec had actual notice of the '739 patent and the infringement alleged herein.

160. Inventec's actions as alleged herein, including those alleged in paragraphs 40-66, constitute induced infringement of at least claim 14 of the '739 patent pursuant to 35 U.S.C. § 271(b).

161. Inventec's actions as alleged herein, including those alleged in paragraphs 40-66, constitute contributory infringement of at least claim 14 of the '739 patent under 35 U.S.C. § 271(c).

162. The above-described acts of direct and induced infringement committed by Inventec have caused injury and damage to ACQIS, and will continue to cause damages and irreparable harm to ACQIS unless enjoined.

163. ACQIS is entitled to recover all damages sustained as a result of Inventec's wrongful acts of infringement, but in no event less than a reasonable royalty pursuant to 35 U.S.C. § 284.

164. Inventec's infringement as described herein has been and continues to be willful and exceptional. Accordingly, ACQIS is entitled to recover enhanced damages up to three times the amount found or assessed at trial pursuant to 35 U.S.C. § 284, as well as its attorneys' fees pursuant to 35 U.S.C. § 285.

COUNT VII
INFRINGEMENT OF RE43,602

165. ACQIS incorporates by this reference the allegations set forth in paragraphs 1 through 164 of this Complaint in support of its seventh cause of action as though fully set forth herein.

166. Pursuant to 35 U.S.C. § 282, the claims of the '602 patent are presumed valid.

167. In view of the foregoing facts and allegations, including paragraphs 13-39 and 59-66 above, Inventec has directly infringed and continues to directly infringe one or more claims of the '602 patent in violation of 35 U.S.C. § 271(a) by making, using, selling, offering to sell, and/or importing the Accused Servers.

168. Inventec's direct infringement of the '602 patent through its manufacture, use, offers to sell, sales, and importation of the Accused Servers is shown by way of the exemplary P47G4 – Single-Socket HPC/AI/VDI Server as set forth in paragraphs 59-66 above, which demonstrates infringement of at least claim 14 of the '602 patent by showing:

(a) the P47G4 – Single-Socket HPC/AI/VDI Server is a system for information transactions:

(b) the P47G4 – Single-Socket HPC/AI/VDI Server comprises a console comprising a power supply connection, and a first low voltage differential signal (LVDS) channel comprising two sets of unidirectional, serial bit channels to convey address and data bits of Peripheral Component Interface (PCI) bus transaction in opposite directions;

(c) the P47G4 – Single-Socket HPC/AI/VDI Server comprises a computer module configured to couple to the console, the computer module comprising a central processing unit (CPU) comprising an interface controller integrated with the CPU as a single chip, a main memory directly coupled to the CPU, a mass storage device directly coupled to the CPU, and a second LVDS channel directly extending from the CPU, the second LVDS channel comprising two sets of unidirectional, serial bit channels to convey data in opposite directions;

(d) wherein the CPU is configured to couple to the console through the second LVDS channel; and

(e) wherein the computer module is configured to receive power from the power supply connection upon coupling of the computer module to the console.

169. ACQIS' infringement allegations against the Accused Servers are not limited to claim 14 of the '602 patent, and additional infringed claims will be identified through infringement contentions and discovery.

170. As early as around May 14, 2018, and at least as of the filing of this Complaint, Inventec had actual notice of the '602 patent and the infringement alleged herein.

171. The above-described acts of direct and induced infringement committed by Inventec have caused injury and damage to ACQIS, and will continue to cause damages and irreparable harm to ACQIS unless enjoined.

172. Inventec's actions as alleged herein, including those alleged in paragraphs 59-66, constitute induced infringement of at least claim 14 of the '602 patent pursuant to 35 U.S.C. § 271(b).

173. Inventec's actions as alleged herein, including those alleged in paragraphs 59-66, constitute contributory infringement of at least claim 14 of the '602 patent under 35 U.S.C. § 271(c).

174. ACQIS is entitled to recover all damages sustained as a result of Inventec's wrongful acts of infringement, but in no event less than a reasonable royalty pursuant to 35 U.S.C. § 284.

175. Inventec' infringement as described herein has been and continues to be willful and exceptional. Accordingly, ACQIS is entitled to recover enhanced damages up to three times the amount found or assessed at trial pursuant to 35 U.S.C. § 284, as well as its attorneys' fees pursuant to 35 U.S.C. § 285.

COUNT VIII
INFRINGEMENT OF RE42,984

176. ACQIS incorporates by this reference the allegations set forth in paragraphs 1 through 175 of this Complaint in support of its eight cause of action as though fully set forth herein.

177. Pursuant to 35 U.S.C. § 282, the claims of the '984 patent are presumed valid.

178. In view of the foregoing facts and allegations, including paragraphs 13-39 and 40-66 above, Inventec has directly infringed and continues to directly infringe one or more claims of the '984 patent in violation of 35 U.S.C. § 271(a) by making, using, selling, offering to sell, and/or importing the Accused Servers.

179. Inventec's direct infringement of the '984 patent through its manufacture, use, offers to sell, sales, and importation of the Accused Servers is shown by way of the exemplary K888G4 – Performance Server System as set forth in paragraphs 40-66 above, which demonstrates infringement of at least claim 40 of the '984 patent by showing:

(a) The K888G4 – Performance Server System is a computer system:

(b) the K888G4 – Performance Server System comprises a console;

(c) the console of the K888G4 – Performance Server System comprises a power supply and a first low voltage differential signal channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions;

(d) the K888G4 – Performance Server System comprises a computer module coupled to the console;

(e) the computer module of the K888G4 – Performance Server System comprises a central processing unit to operate on a varying clock frequency to vary a power consumption of the central processing unit while in operation;

(f) the computer module of the K888G4 – Performance Server System comprises a mass storage unit coupled to the central processing unit;

(g) the computer module of the K888G4 – Performance Server System comprises a second low voltage differential signal channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions;

(h) the computer module of the K888G4 – Performance Server System comprises a peripheral bridge directly coupled to the central processing unit without any intervening Peripheral Component Interconnect bus, the peripheral bridge comprising an interface controller to output a serial bit stream that is conveyed over the second low voltage differential signal channel;

(i) wherein the interface controller of the K888G4 – Performance Server System is coupled to the console through the second low voltage differential signal channel; and

(j) wherein the computer module of the K888G4 – Performance Server System is configured to receive power from the power supply.

180. ACQIS' infringement allegations against the Accused Servers are not limited to claim 40 of the '984 patent, and additional infringed claims will be identified through infringement contentions and discovery.

181. As early as around May 14, 2018, and at least as of the filing of this Complaint, Inventec had actual notice of the '984 patent and the infringement alleged herein.

182. Inventec's actions as alleged herein, including those alleged in paragraphs 40-66, constitute induced infringement of at least claim 14 of the '984 patent pursuant to 35 U.S.C. § 271(b).

183. Inventec's actions as alleged herein, including those alleged in paragraphs 40-66, constitute contributory infringement of at least claim 14 of the '984 patent under 35 U.S.C. § 271(c).

184. The above-described acts of direct and induced infringement committed by Inventec have caused injury and damage to ACQIS, and will continue to cause damages and irreparable harm to ACQIS unless enjoined.

185. ACQIS is entitled to recover all damages sustained as a result of Inventec's wrongful acts of infringement, but in no event less than a reasonable royalty pursuant to 35 U.S.C. § 284.

186. Inventec's infringement as described herein has been and continues to be willful and exceptional. Accordingly, ACQIS is entitled to recover enhanced damages up to three times the amount found or assessed at trial pursuant to 35 U.S.C. § 284, as well as its attorneys' fees pursuant to 35 U.S.C. § 285.

JURY TRIAL DEMANDED

ACQIS LLC, hereby demands a trial by jury on all claims and issues so triable.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff ACQIS LLC respectfully requests that this Court grant the following relief to ACQIS LLC:

A. enter judgment that Inventec has infringed, both directly and indirectly, one or more claims of each of the ACQIS Patents and continues to infringe those claims through: (1) the manufacture, use, offering to sale, and/or sale in the United States, and/or the importation into the United States, of infringing computer products; (2) the practice of claimed methods of the ACQIS Patents by using and/or testing computer products in the United States; (3) the importation into the United States of computer products made abroad using ACQIS's patented processes; and (4) the

inducement of third parties to engage in, and/or contributing to the engagement of third parties in, the activity described above with knowledge of the ACQIS Patents and of the third parties' infringing actions;

B. enter judgment that such infringement is willful;

C. enter judgment awarding ACQIS monetary relief pursuant to 35 U.S.C. § 284 in an amount adequate to compensate for Inventec's infringement of the ACQIS Patents to be determined at trial, but not less than a reasonable royalty, awarding ACQIS all pre- and post-judgment interest and costs, and awarding ACQIS enhanced damages for Inventec's willful infringement of the ACQIS Patents;

D. enter an order that Inventec pay to ACQIS ongoing royalties in an amount to be determined for any infringement occurring after the date that judgment is entered;

E. enter an order, pursuant to 35 U.S.C. § 285, declaring this an exceptional case and awarding to ACQIS its reasonable attorneys' fees; and

F. enter an order awarding to ACQIS such other and further relief, whether at law or in equity, that this Court seems just, equitable, and proper.

Dated: October 15, 2020.

Respectfully submitted,

By: */s/ Paige Arnette Amstutz*

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